

Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size

Document Number

LZ57

Rev

-1

Date:

Tuesday, March 29, 2011

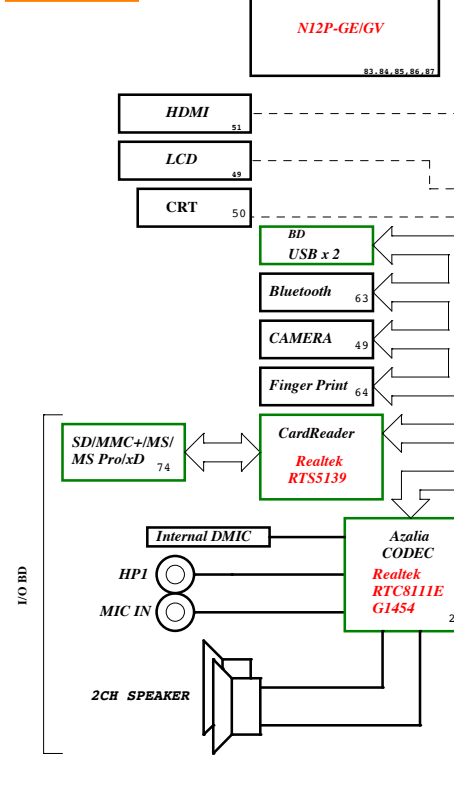
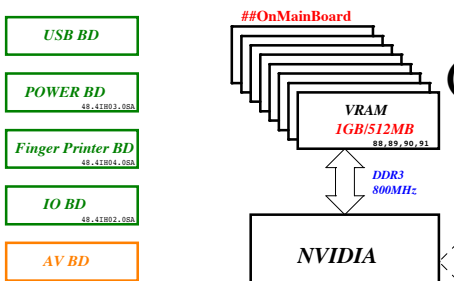
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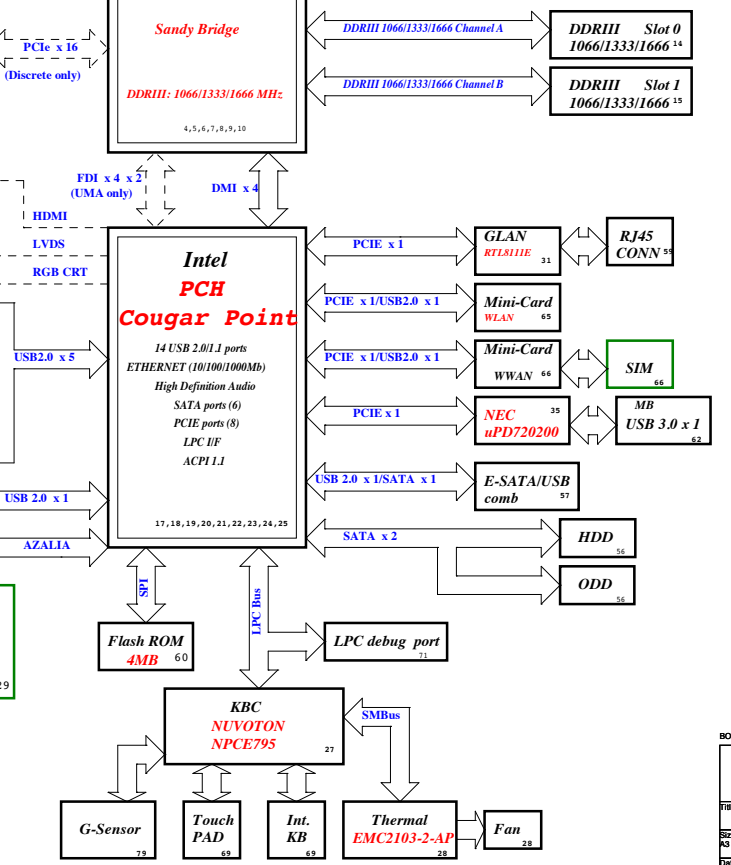
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100

Block Diagram (UMA/Optimus co-lay)



Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC



SYSTEM DC/DC		CPU DC/DC	
RT8208B 48		NCP6131 42-44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	OD5V_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC		SYSTEM DC/DC	
UP6111CQHC 45		UP6183AQAG 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_VTT	5V_AUX_S5	3D3V_AUX_S5
		5V_S5	3D3V_S5
SYSTEM DC/DC		SYSTEM DC/DC	
UP6111C 46		NCP5911 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3	DCBATOUT	VCC_GFXCORE
	DDR_VREF_S3		
SYSTEM DC/DC		SYSTEM DC/DC	
RT8208B 92		BQ24745 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	+DC_IN_S5	DCBATOUT
		+PRATT	
SYSTEM DC/DC		SYSTEM DC/DC	
RT9025 47		G9091-180T11U 24, 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_S0	3D3V_S5	1D5V_S5
		3D3V_S0	1D8V_VGA_S0
SYSTEM DC/DC		SYSTEM DC/DC	
RT9026 46		L757 1	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	0D75V_S0		
PCB LAYER		PCB LAYER	
L1:Top	L5:VCC	L1:Top	L5:VCC
L2:GND	L6:Signal	L2:GND	L6:Signal
L3:Signal	L7:GND	L3:Signal	L7:GND
L4:Signal	L8:Signal	L4:Signal	L8:Signal

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<p>PCH Strapping</p>	<p>Processor Strapping</p>		
<p>Huron River Schematic Checklist Rev.0 7</p>	<p>Huron River Schematic Checklist Rev.0 7</p>		

Name	Schematics Notes	Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
SPKR	Reboot option at power-up. Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ	CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
INIT3_3V#	Weak internal pull-up resistor. Weak internal pull-up. Leave as "No Connect".	CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: connected to the EMBEDDED display Port	0
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.	CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.	CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESET# de assertion 0: PEG Wait for BIOS for training	
NV_ALE	Enable Danbury: Connect to +MVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)				
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.				
HAD_DOCK_EN# [GPIO33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measures defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for PD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.				
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.				
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.				
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.				
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.				
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.				

POWER PLANE		VOLTAGE	Voltage Rails	DESCRIPTION
			ACTIVE IN	
SV_S0	SV	1.5V		
3DV3_S0	3.3V	1.8V		
10DV_S0	1.0V	0.9V - 0.85V		
10DV_VTT	1.05V	0.75V		
10DV_S0	0.9V - 0.85V	0.25V to 1.5V	S0	
007SV_S0	0.75V	0.4 to 1.25V		
VCC_CORE	0.25V to 1.5V	1.8V		CPU Core Rail
VCC_SFACORE	0.4 to 1.25V	1.3V		Graphics Core Rail
10DV_VGA_S0	1.0V	1V		
3DV3_VGA_S0	3.3V			
1V_VGA_S0	1V			
SV_DBG#_S3	SV	1.5V	S3	
DDR_VREF#_S3	0.75V			
BP#	6V-14.1V			
DCRATOUT	6V-14.1V			AC Brick Mode only
SV_S5	SV	All 8 states		
SV_AUX_S5	SV			
3DV3_S5	3.3V			
3DV3_AUX_S5	3.3V			
3DV3_IAN_S5	3.3V	WOL_EN		Legacy WOL
3DV3_AUX_FRC	3.3V	DSM, Sx		OS for supporting Deep Sleep states
3DV3_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and v34L16 Sx

USB Table

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card


SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (MWMAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	MURCON RIVER OMB		
Device		Address	Hex	Bus
IC SMBus 1				BAT_RCL/BAT_SDA
Battery CHARGER				BAT_RCL/BAT_SDA
				BAT_RCL/BAT_SDA
IC SMBus 2				SW1_CLK/SW1_DATA
PCB				SW1_CLK/SW1_DATA
eDP				SW1_CLK/SW1_DATA
PCH SMBus				PCH_SMBDATA/PCH_SMBIO
SO-DIMM (SPD)				PCH_SMBDATA/PCH_SMBIO
SO-DIMM (SPD)				PCH_SMBDATA/PCH_SMBIO
Digital Pot				PCH_SMBDATA/PCH_SMBIO
G-Sensor				PCH_SMBDATA/PCH_SMBIO
MINI				PCH_SMBDATA/PCH_SMBIO

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Title	
<div> CPU (PCIe/DMI/FDI) LZ57 </div>	
Size A3	<div> Document Number Rev -1 </div>
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SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistor (power (~15 mW) may be
wasted).

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

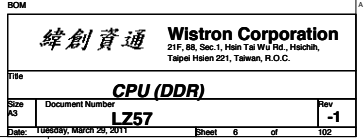
20100722 follow Astro add buffer

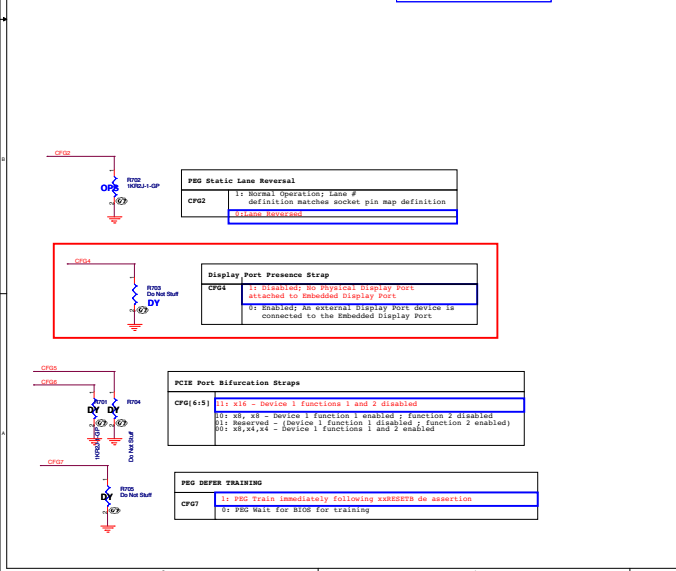
20100722 SA confirm.

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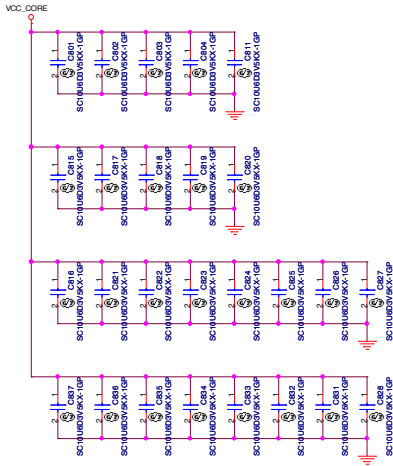


SSID = CPU

POWER

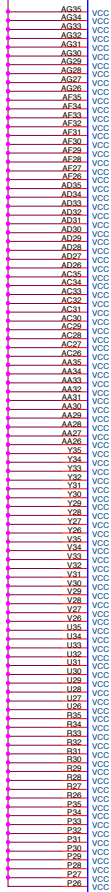
PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE



SANDY

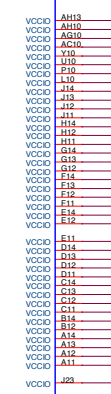
CORE SUPPLY

SVID

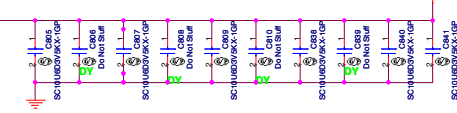
SENSE LINES

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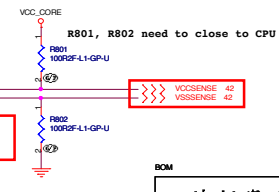
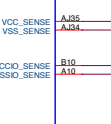
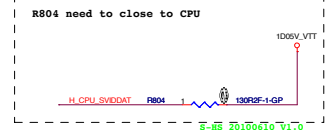
PEG AND DDR



VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

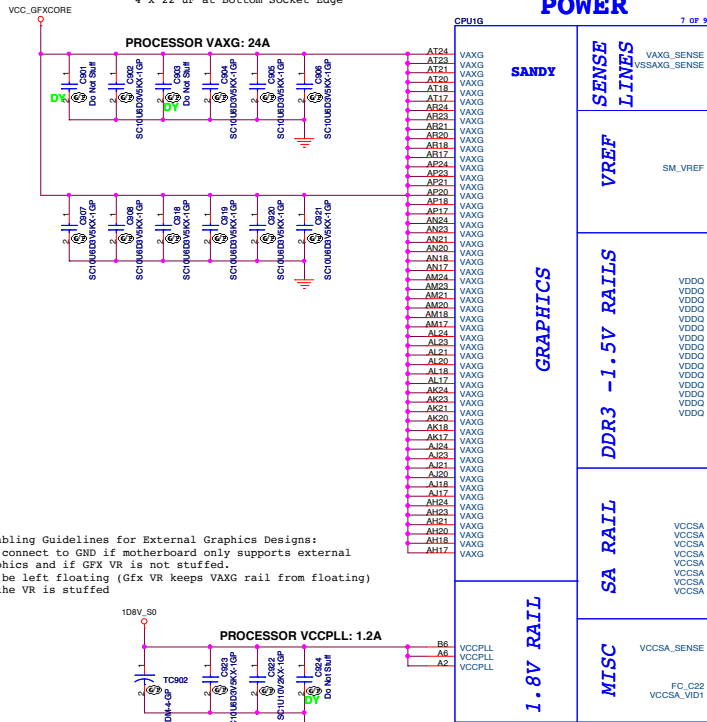


No-stuff sites inside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.



SSID = CPU

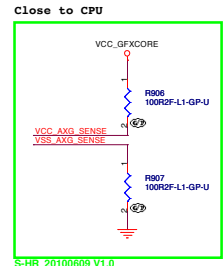
VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge



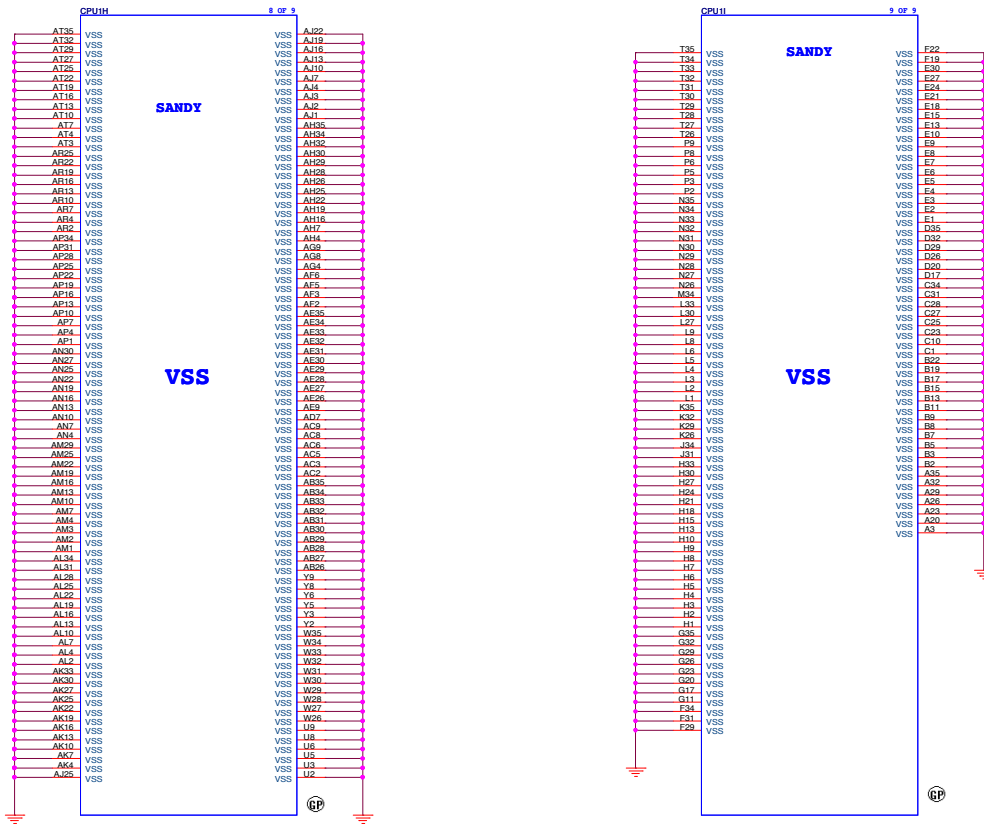
Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

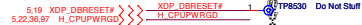
+V_SM_VREF_CNT should have 10 mil trace width

Routing Guideline:
Power from DDR VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.



20100721 standard schematic update





CAD Note: The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net.

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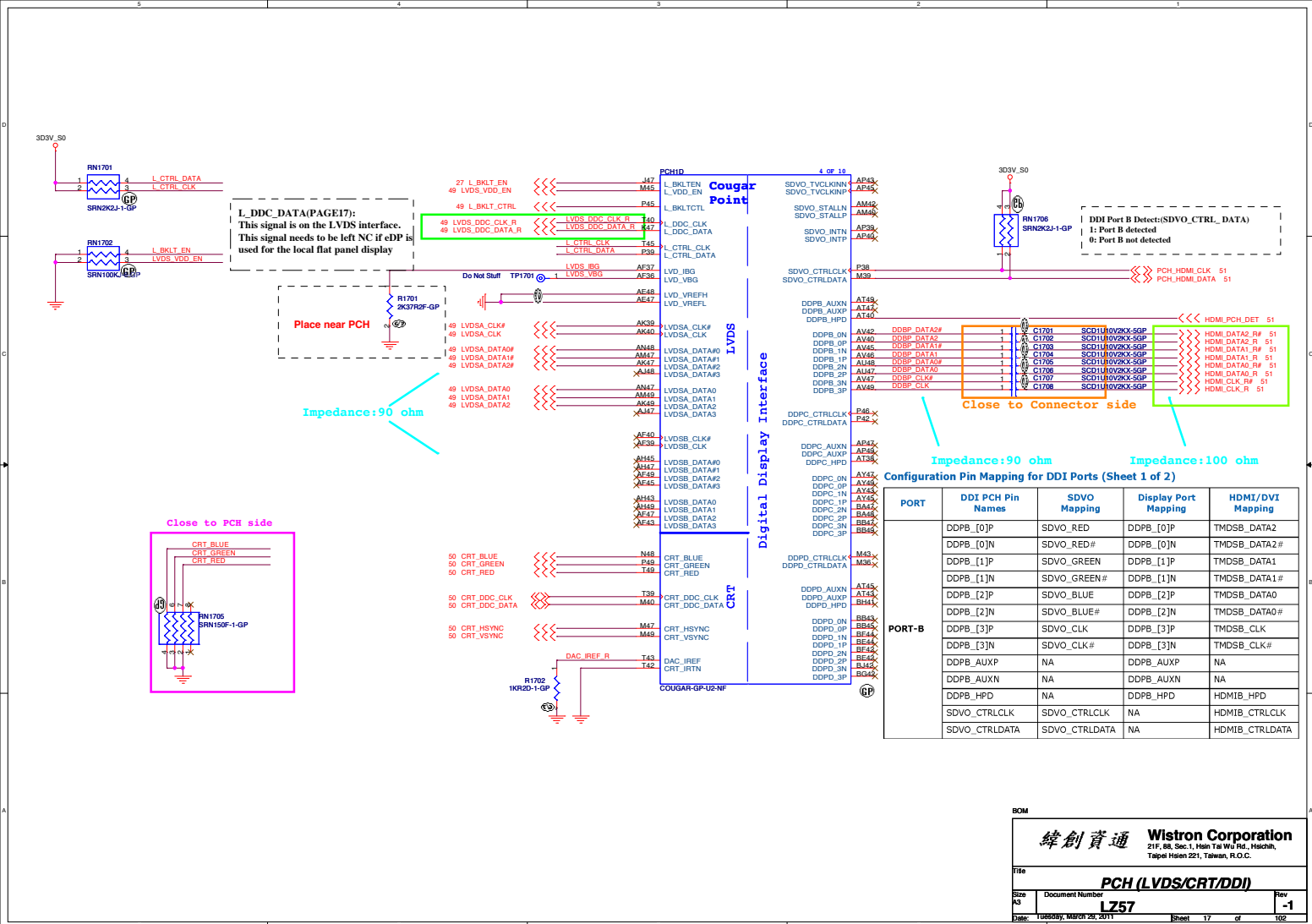
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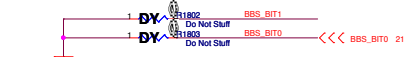
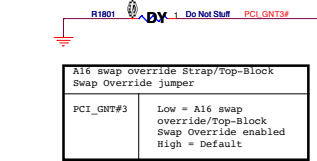
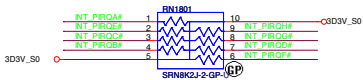
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Size A4	Document Number LZ57	Rev -1
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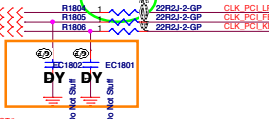
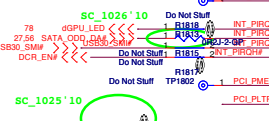
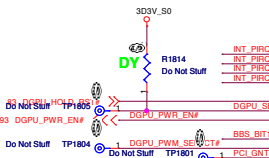
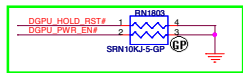


SSID = PCH

20100725 Annie modify



BOOT BIOS Strap	
ENT1#/GPIO1	SATA1G#/GPIO19
0	0
0	1
1	0
1	1



Cougar Point

RSVD

NVDRAM

USB

PCI

COUGAR-UP2-NF

USB

USB

USB

USB

USB

USB

USB

USB

RSVD

NVDRAM

USB

PCI

COUGAR-UP2-NF

USB

USB

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RSVD

NVDRAM

USB

PCI

COUGAR-UP2-NF

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RSVD

NVDRAM

USB

PCI

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USB

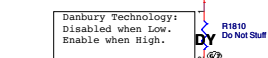
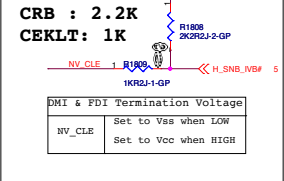
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USB

USB

USB

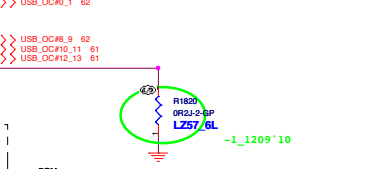
USB



USB Ext. port 1 (HS)
External debug port use on Huron river platform

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD)
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (MLAN)
12	CAMERA
13	X

SW programming USB_OC#12_13 for USB 9



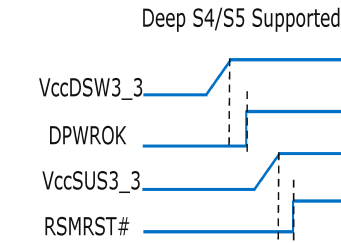
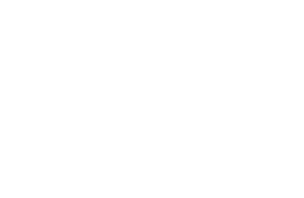
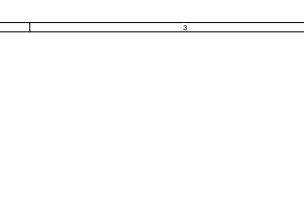
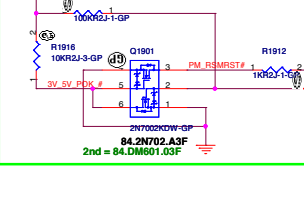
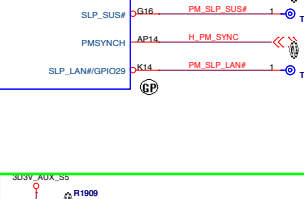
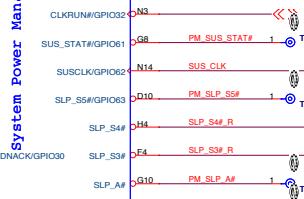
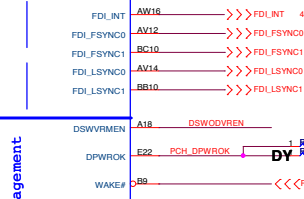
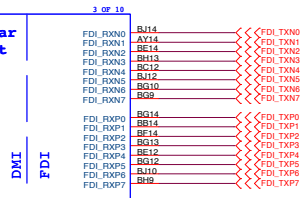
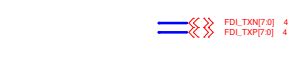
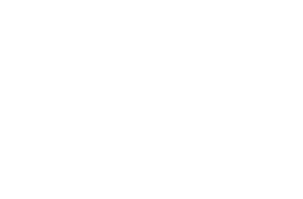
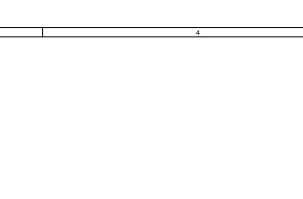
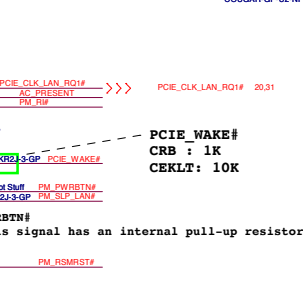
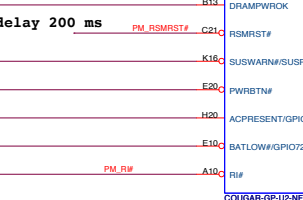
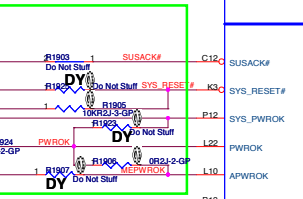
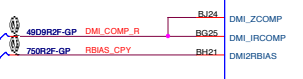
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 321, Taiwan, R.O.C.

File: PCH (PCI/USB/NVDRAM)
Size: A3
Document Number: LZ57
Date: Tuesday, March 29, 2011
Sheet: 18 of 102
Rev: -1

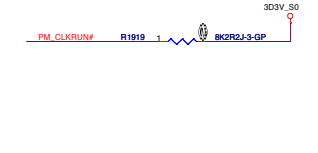
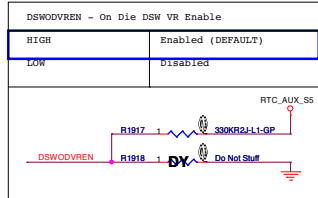
SSID = PCH



Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWDRNACK/GPIO30



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

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PCH (DM I/FD/PM)
LZ57

Rev -1

Date: Tuesday, March 29, 2011

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100

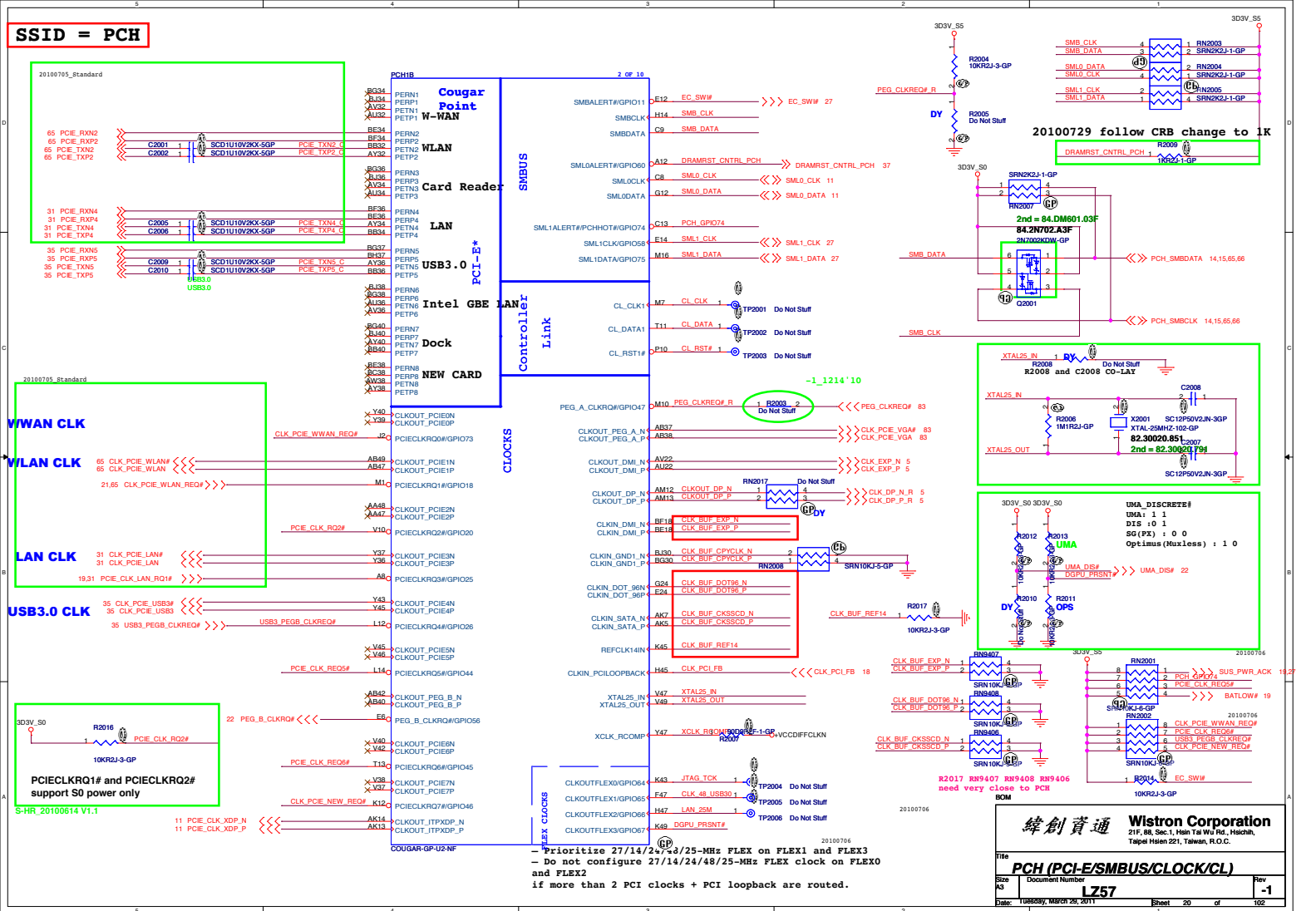
100

100

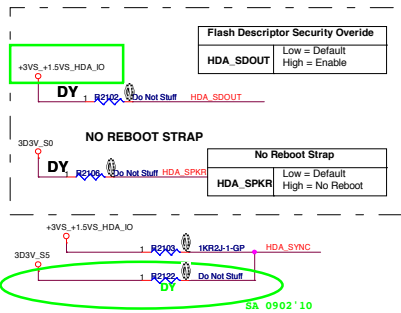
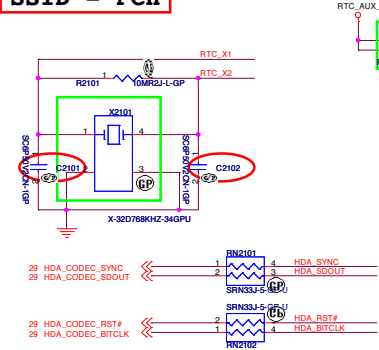
100

100

SSID = PCH

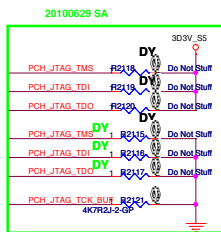
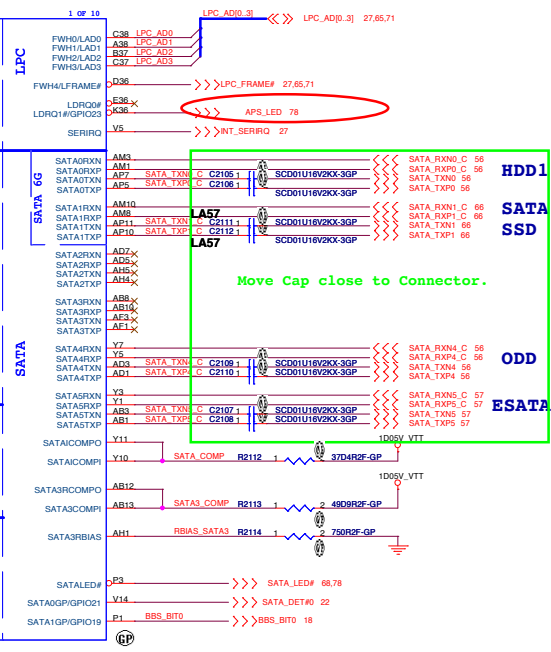
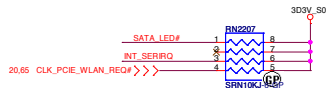
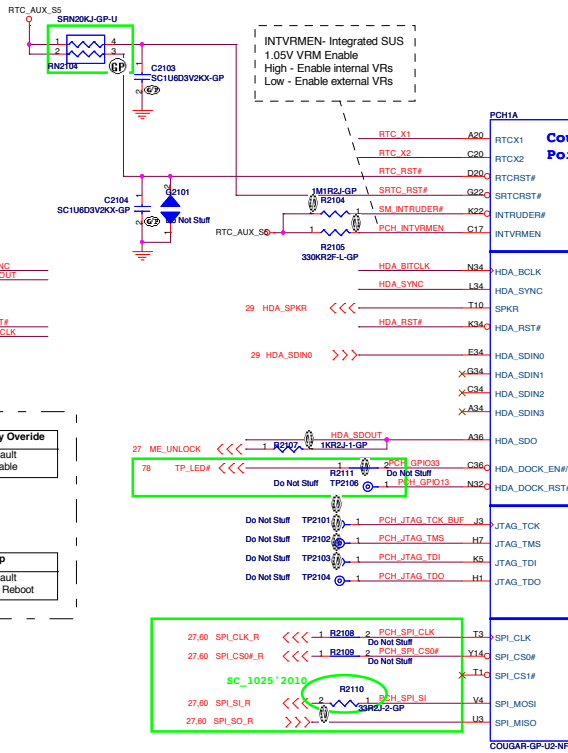


SSID = PCH



This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



Note:
For PCH debug with XDP, need to NO STUFF R2218

3.3V_S0

R2205
Do Not Stuff

DY

U1A, CRB_DET

R2206
100KR2J-1-GP

20 PEG_B_CLKREQ# <<<<

PCH GPIO24 1

PCH GPIO12 2

USB3 PWR_ON 3

4

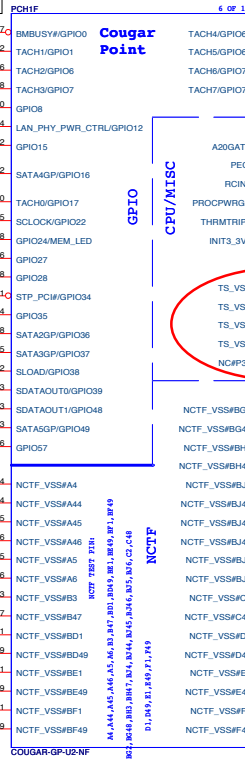
SRN10K

PLL_ODVR_EN 2

PCH GPIO15 1

10KRF2

10KRF2



PLL ON DIE VR ENABLE

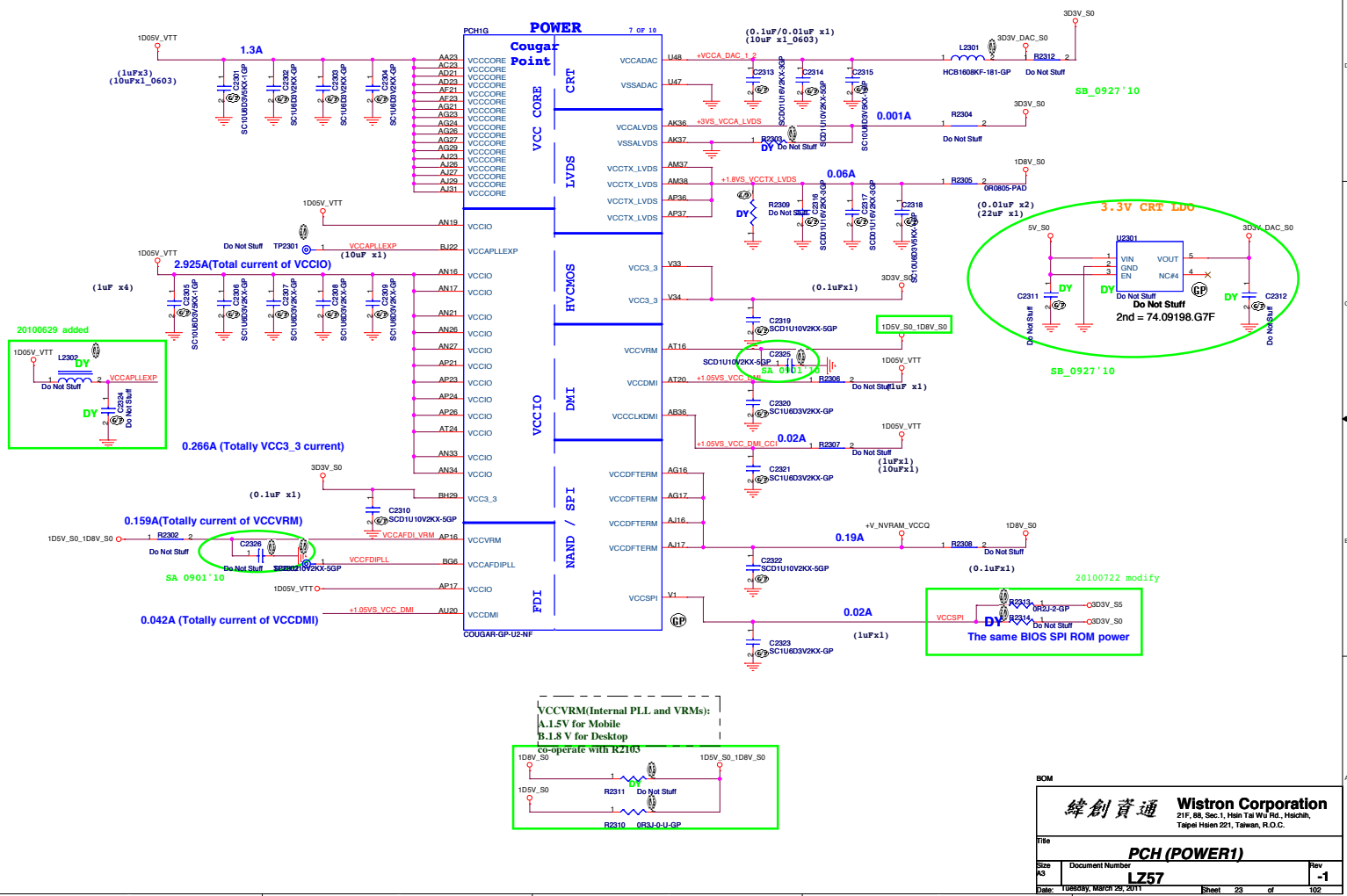
NOTE: This signal has a weak internal pull-up
20K

ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN **DY** 1 R2212

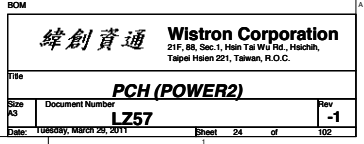
GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

BOM		緯創資通 Wistron Corporation 21F, 88C, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PCH (GPIO/CPU) L757			
Size A3	Document Number		Rev -1
Date:	Tuesday, March 25, 2014	Sheet 22	of 102

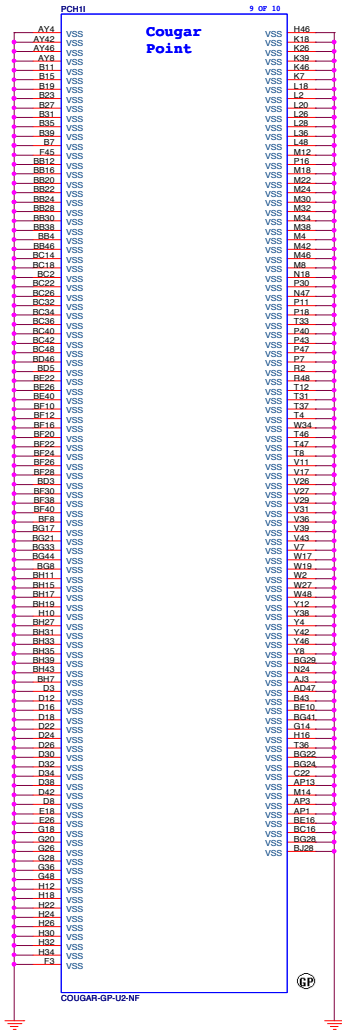
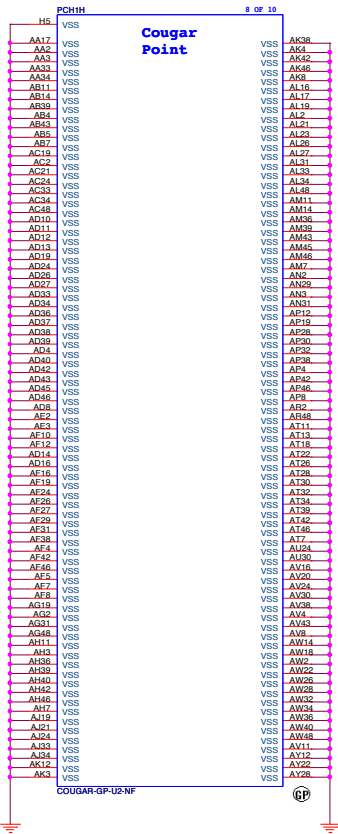


[illegible]

RTC	CPU
Clock and Miscellaneous	



SSID = PCH



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File

Size A3

Document Number

PCH (VSS)

Date: Tuesday, March 29, 2011

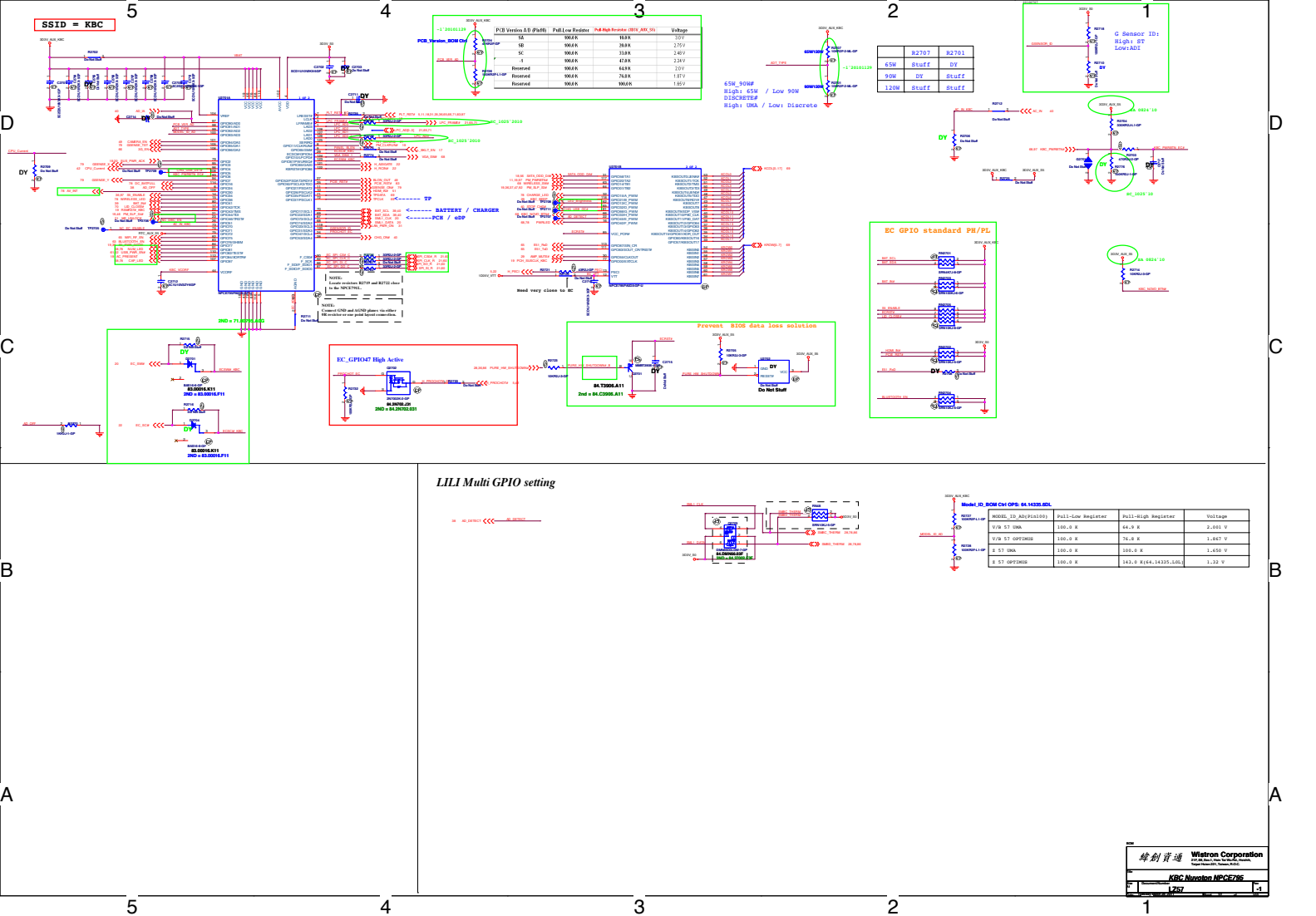
Sheet 25 of 102

Rev -1

(Blanking)

BOM

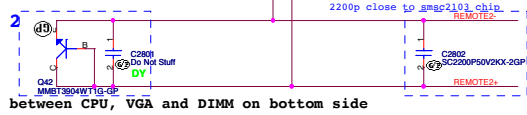
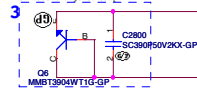
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div> <div>Reserved</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>LZ57</div>		<div>Rev</div> <div>-1</div>
<div>Date: Tuesday, March 29, 2011</div>		<div>Sheet</div> <div>26</div>	<div>of</div> <div>102</div>



SSID = Thermal

Thermal sensor

Close to PCH on top side.

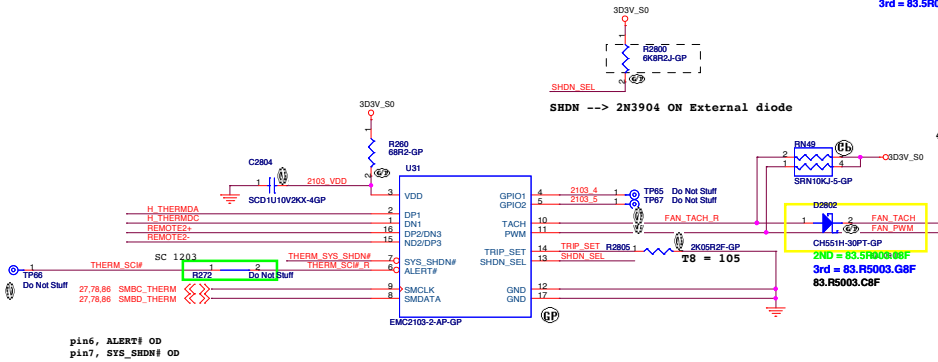


T8

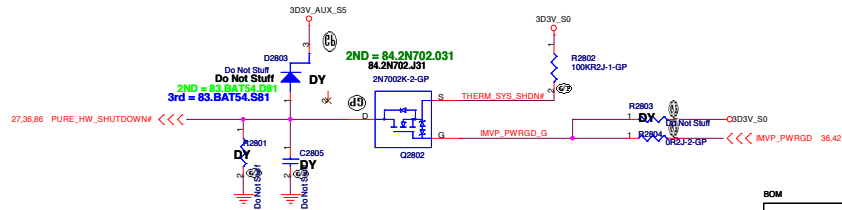


CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

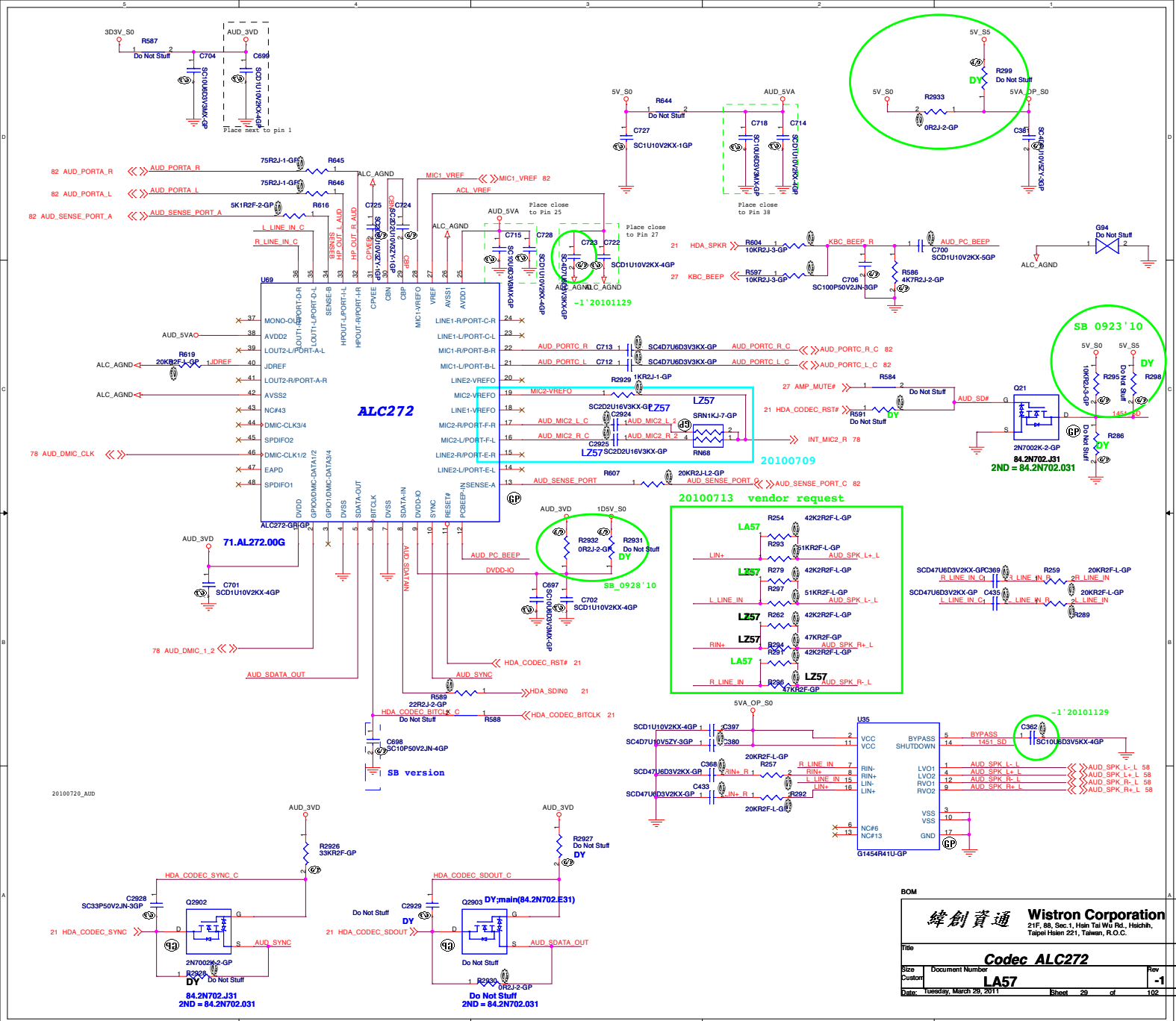


pin6, ALERT# OD
pin7, SYS_SHDN# OD



BOM

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thermal P2800/Fan Controller P2793	
Size A3	Document Number LZ57
Date: Tuesday, March 29, 2011	Sheet 28 of 102



blanking

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>reserved</div>	
Size <div>A4</div>	Document Number <div>LZ57</div>
Date <div>Tuesday, March 29, 2011</div>	Rev <div>-1</div>
Sheet 30 of 102	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		RTS5159 (CARD READER)	
Size	Document Number	Rev.	
A3	LZ57		-1
Date:	Tuesday, March 29, 2011	Sheet	32 of 102

(Blanking)

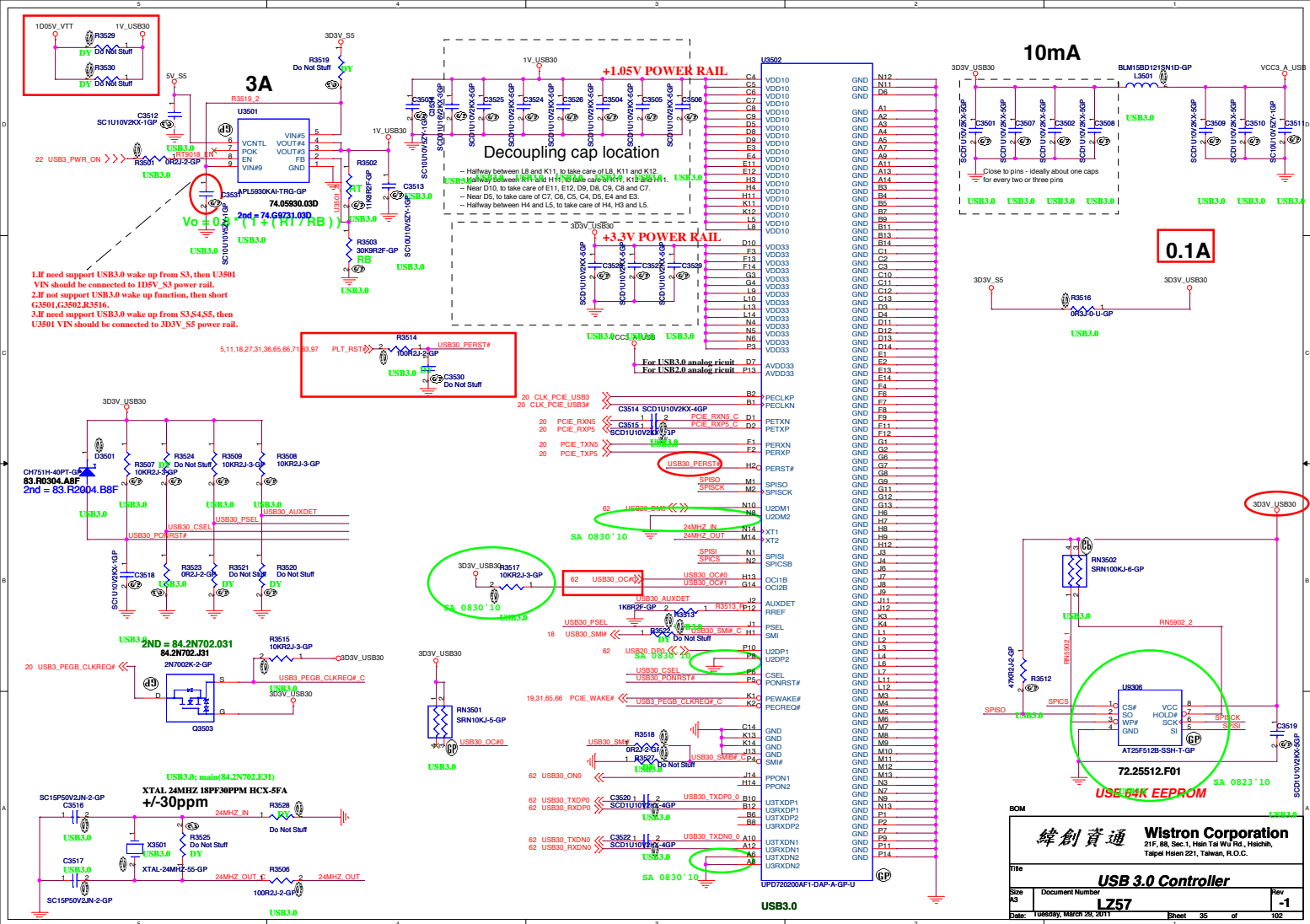
BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Reserved</div>	
Size <div>A4</div>	Document Number <div>LZ57</div>
Date <div>Tuesday, March 29, 2011</div>	Rev <div>-1</div>
Sheet 33 of 102	

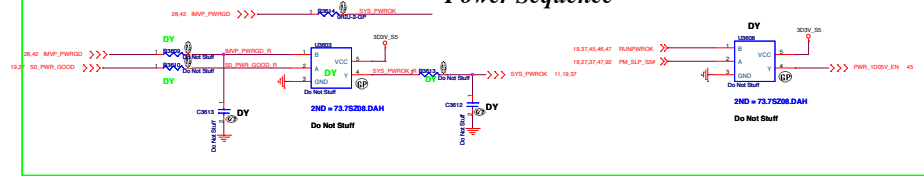
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BOM

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div> <div>Reserved</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>LZ57</div>		<div>Rev</div> <div>-1</div>
<div>Date: Tuesday, March 29, 2011</div>		<div>Sheet</div> <div>34</div>	<div>of</div> <div>102</div>

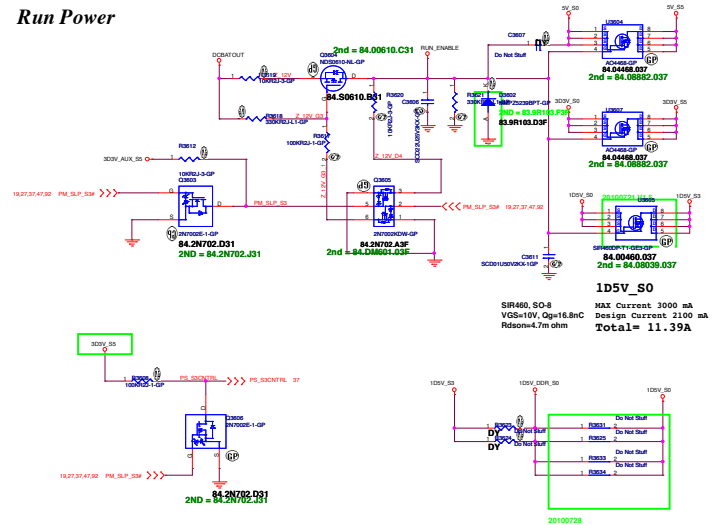


Power Sequence



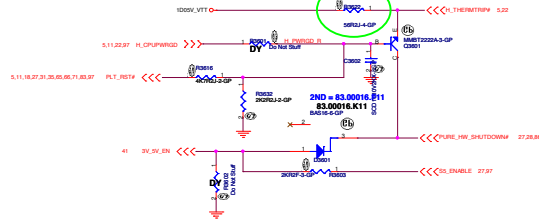
SSID = Reset.Suspend

Run Power

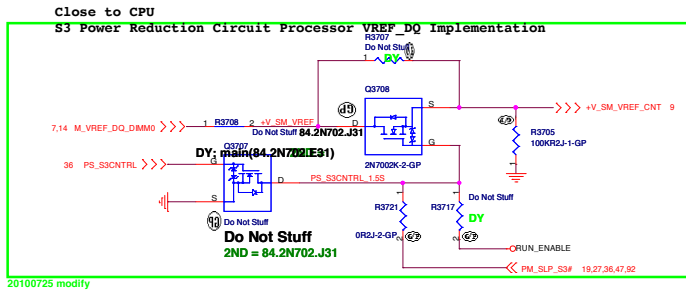


100V_VTT
SIR460, SO-8
VGS=10V, Qg=16.8nC
Rds(on)=4.7m ohm
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

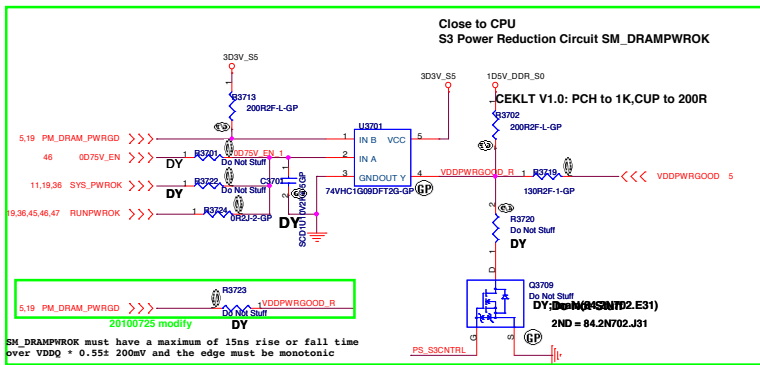
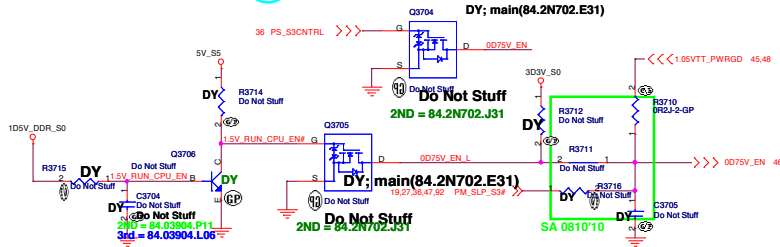
SB 0923'10



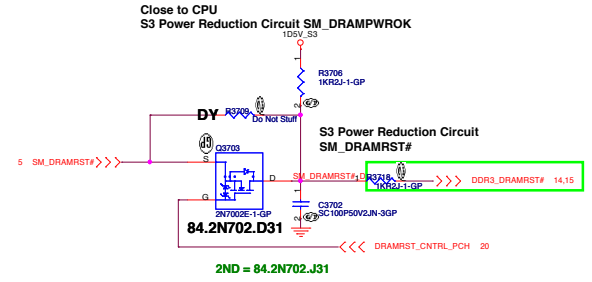
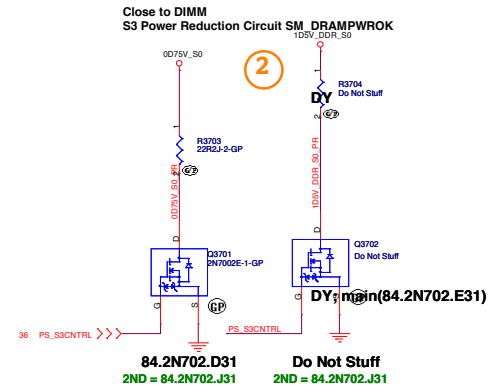
Wistron Corporation	
Power Plane Enable	
Document Number	LZ57
Version	1.0
Page	1 of 1



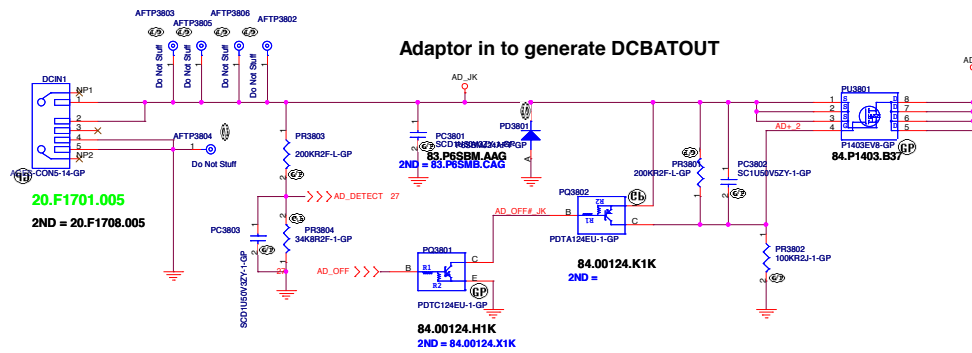
5 S3 Power Reduction X01 20091111



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ + 0.55t 200nsV and the edge must be monotonic



BOM	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
File	ADAPTER
Size	Document Number
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Date	Tuesday, March 24, 2011
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BOM

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
Title	DCIN JACK
Size	Document Number LZ57
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5 4 3 2 1

D

C

B

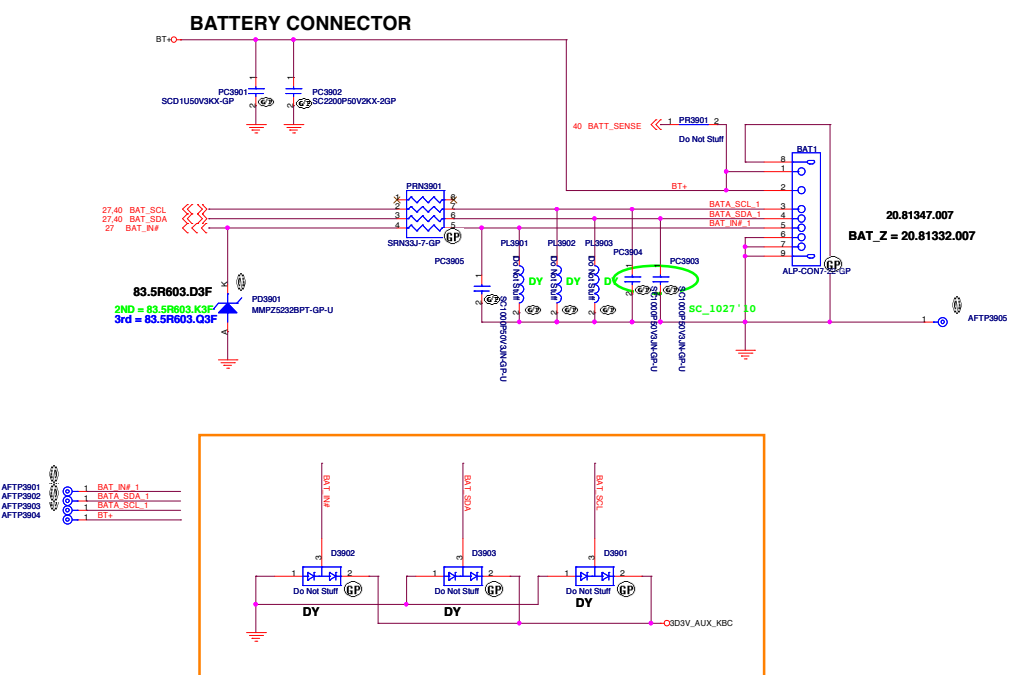
A

D

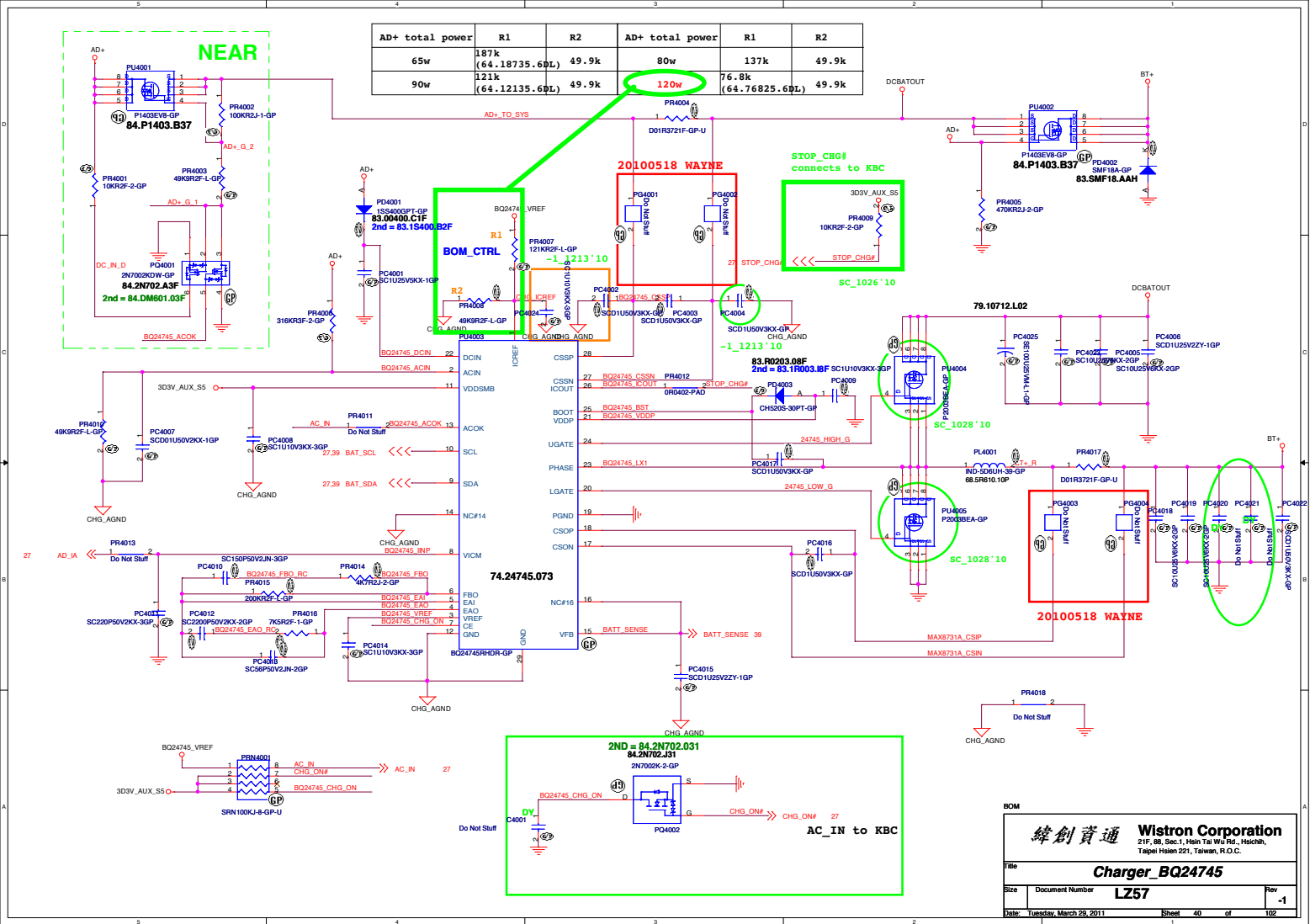
C

B

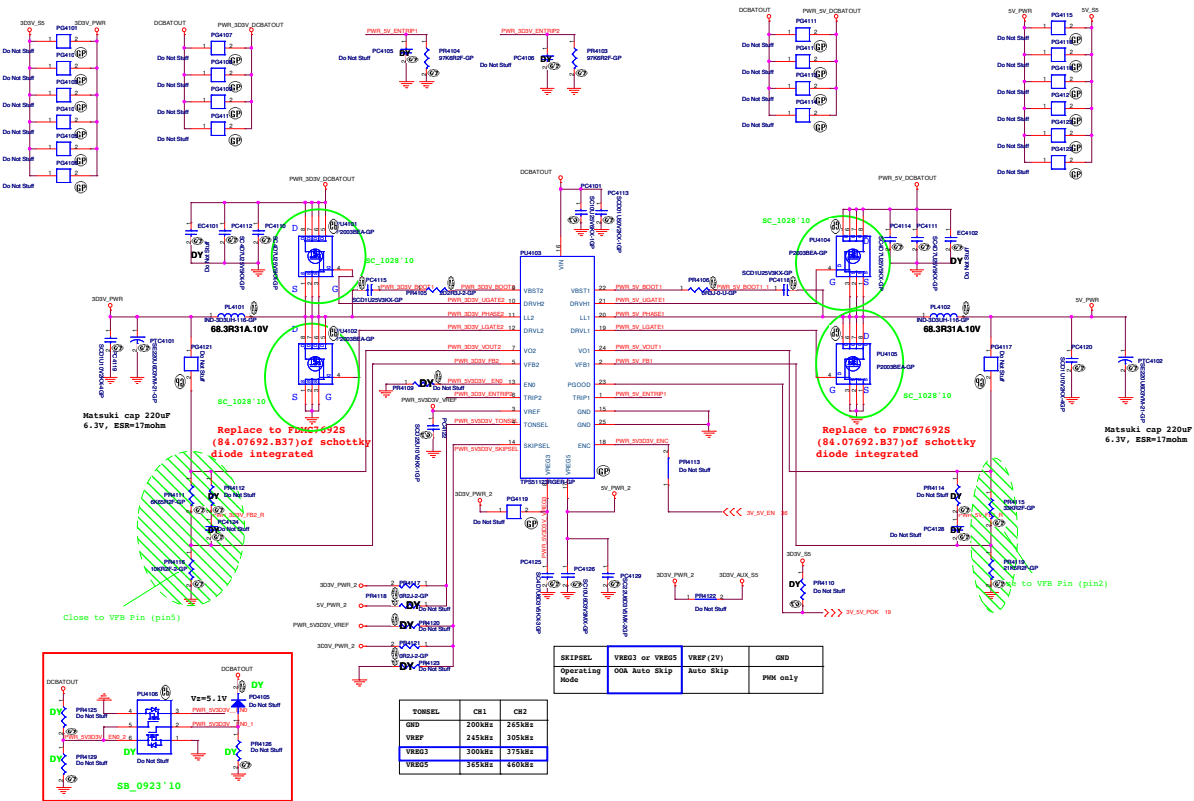
A

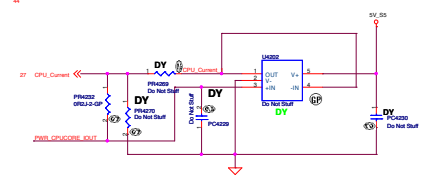


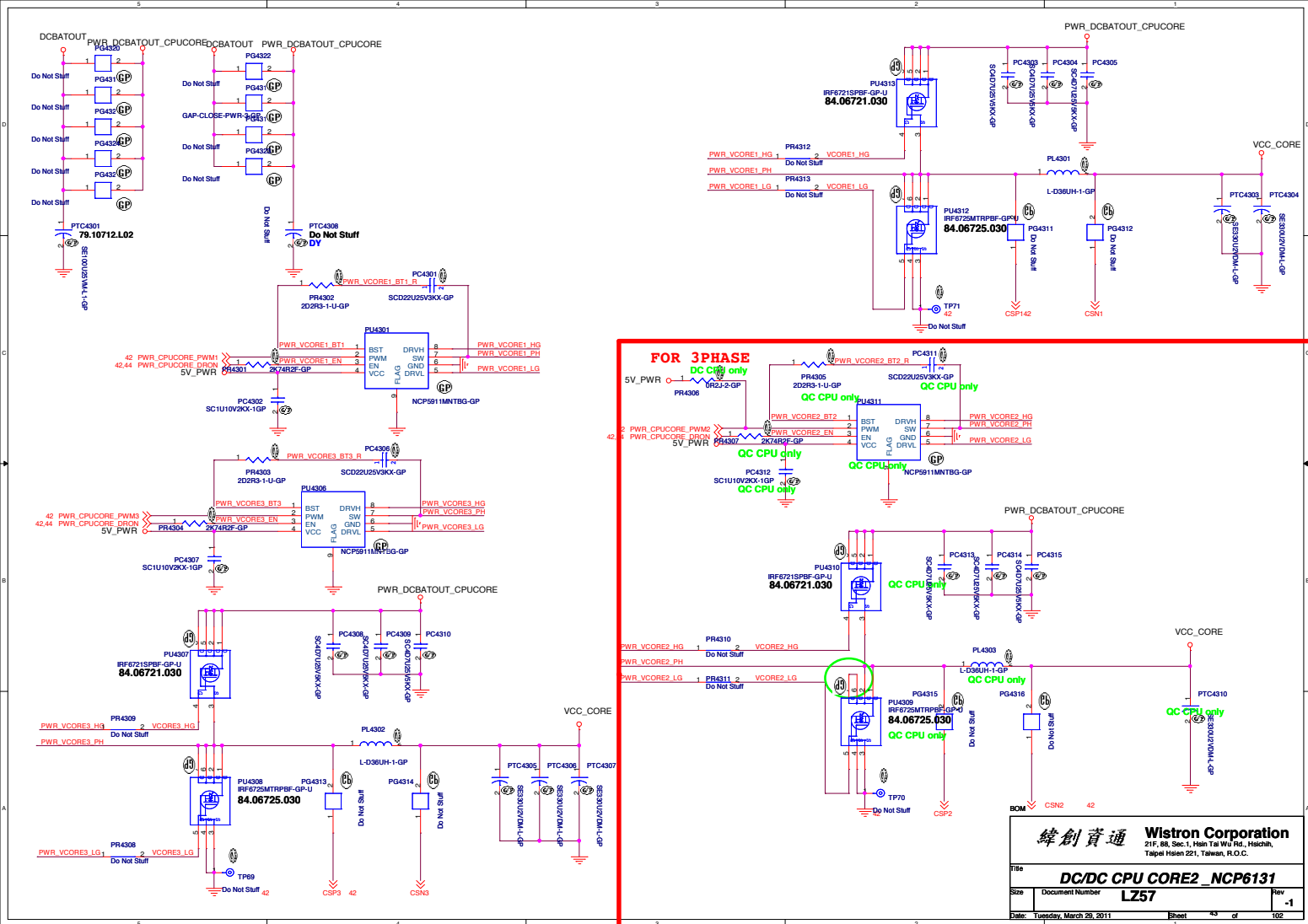
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipen Hsien 221, Taiwan, R.O.C.	
File	BATT_CONN
Size	Document Number LZ57
Date: Tuesday, March 29, 2011	Sheet 99 of 102
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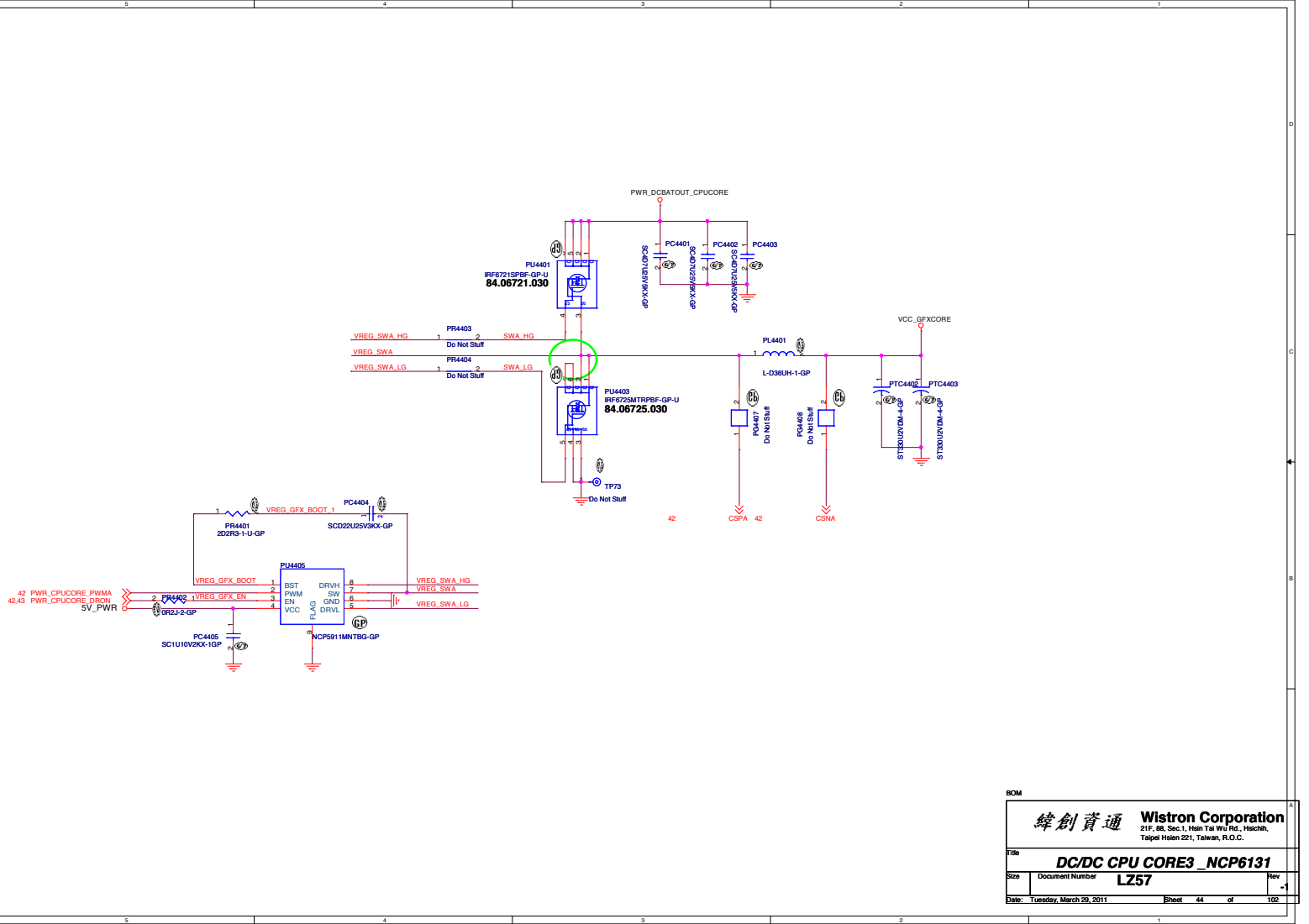


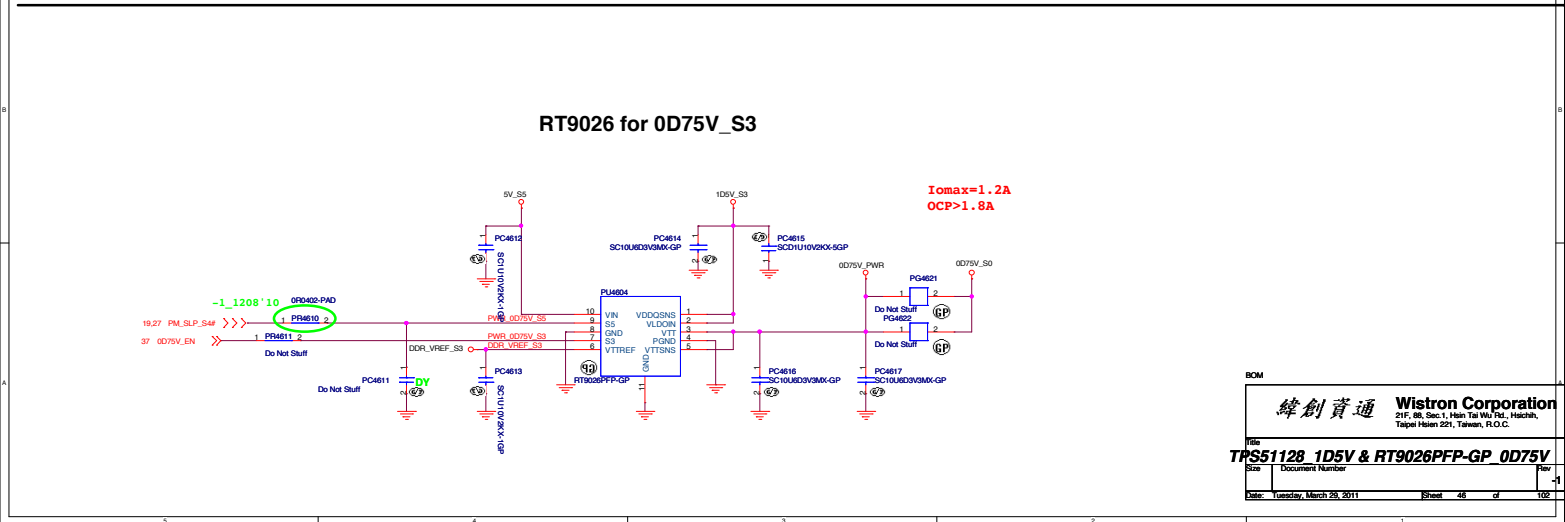
SSID = PWR.Plane.Regulator_5v3p3v





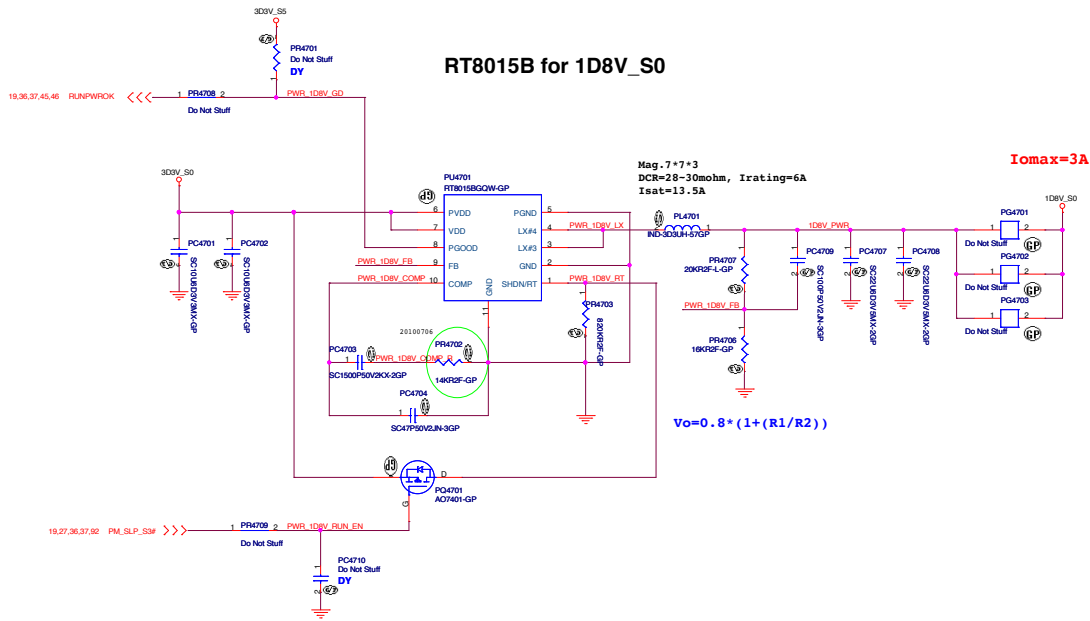






RT9025 for 1D8V_S0

RT8015B for 1D8V_S0

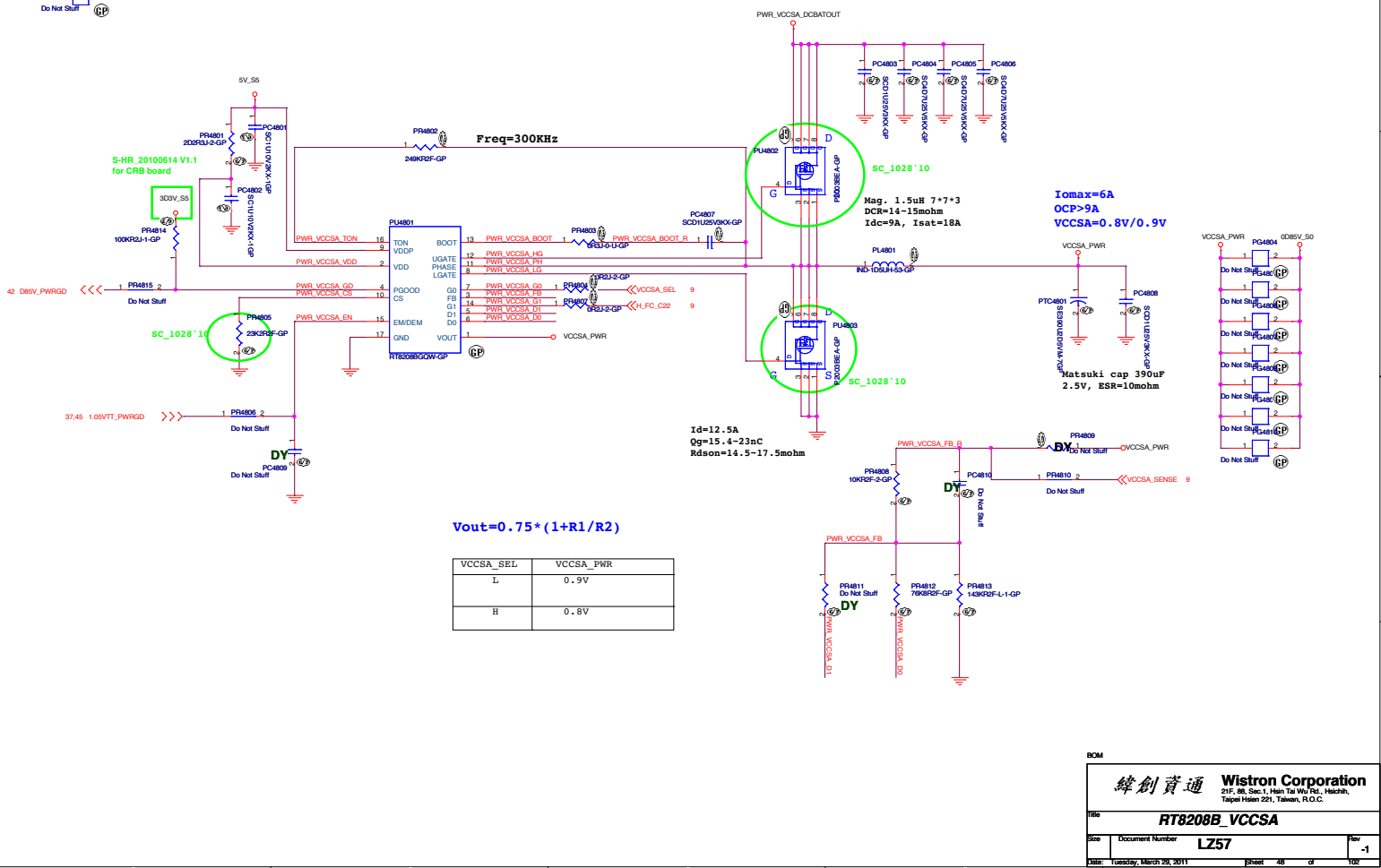


BCM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 301, Taiwan, R.O.C.

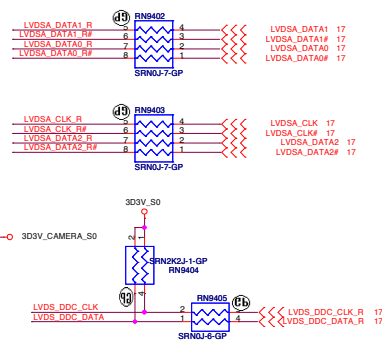
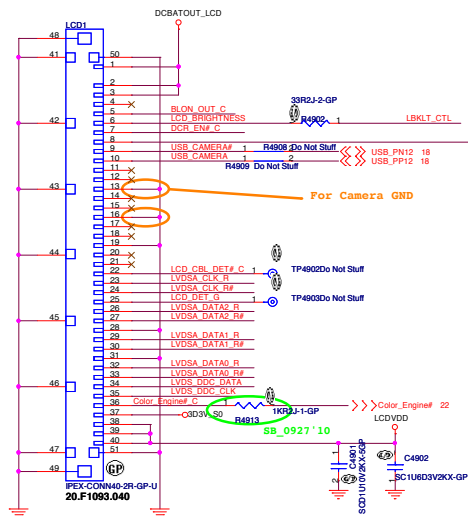
File	1D8V_RT9025		
Size	Document Number	LZ57	Rev -1
Date	Tuesday, March 28, 2011	Sheet 27	of 102

RT8208A for VCCSA

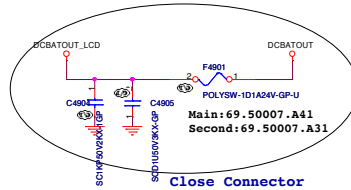
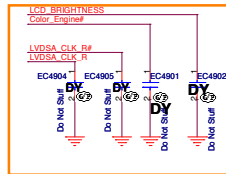


VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

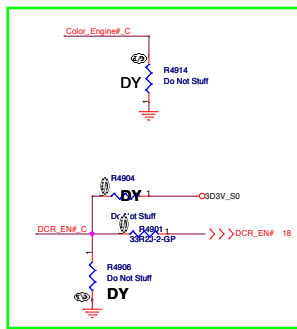
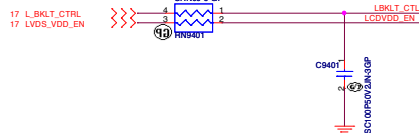
LVDS CONNECTOR



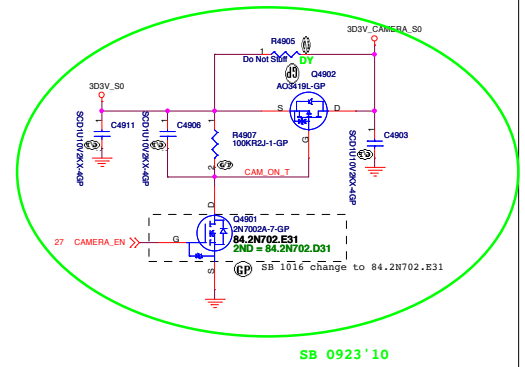
For EMI request
Close to LVDS connector



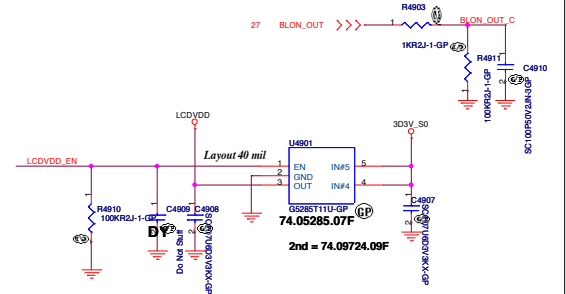
Panel BL brightness/Power En/BL En



CAMERA POWER



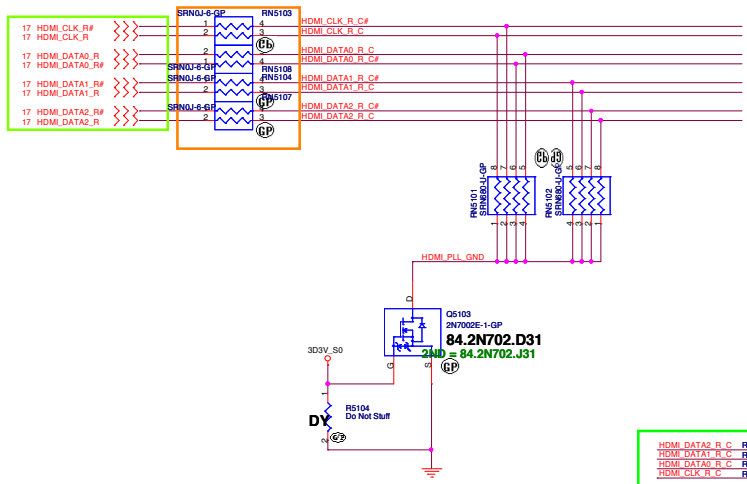
SSID = VIDEO



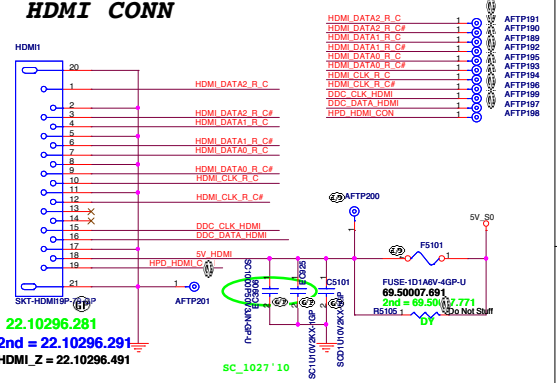
BOM		 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LCD Connector	
Size A3	Document Number	Rev -1	
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HDMI Passive Level Shifter

Close to HDMI Connector

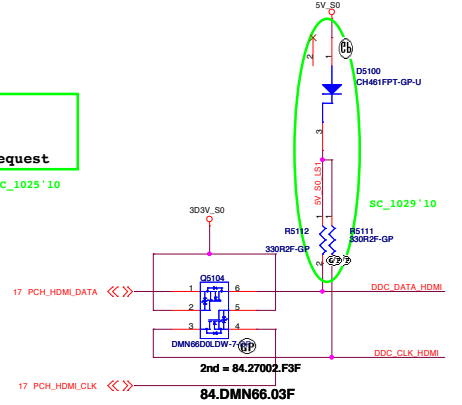
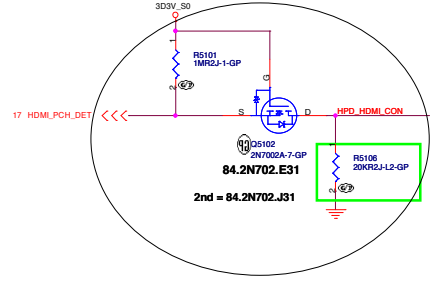
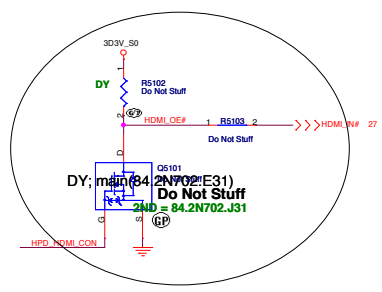


HDMI DDC Passive Level Shifter



20100727 modify, KBC isn't use.

20100727 follow intel design guide



(Blanking)

(Blanking)

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>S-VIDEO</div>	
Size <div>A4</div>	Document Number <div>LZ57</div>
Rev <div>-1</div>	
Date: Tuesday, March 29, 2011	
Sheet 53 of 102	

(Blanking)

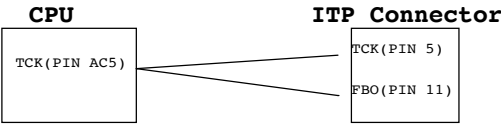
BOM

緯創資通		Wistron Corporation	
21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LZ57		-1
Date:	Tuesday, March 29, 2011		Sheet 54 of 102
2	1		

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

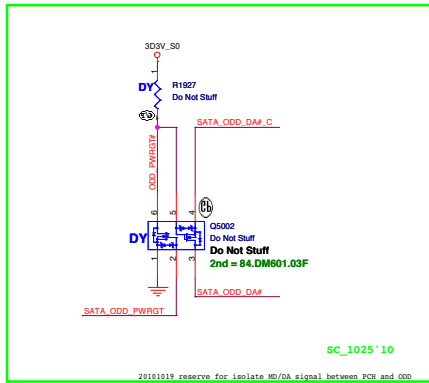
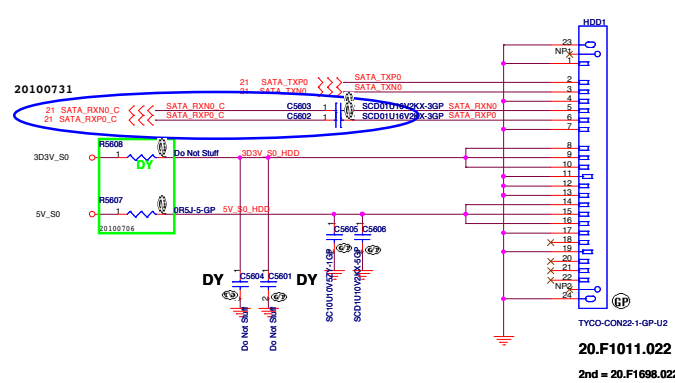


BOM

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
TitleITP		
SizeA4	Document NumberLZ57	Rev-1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

SSID = SATA

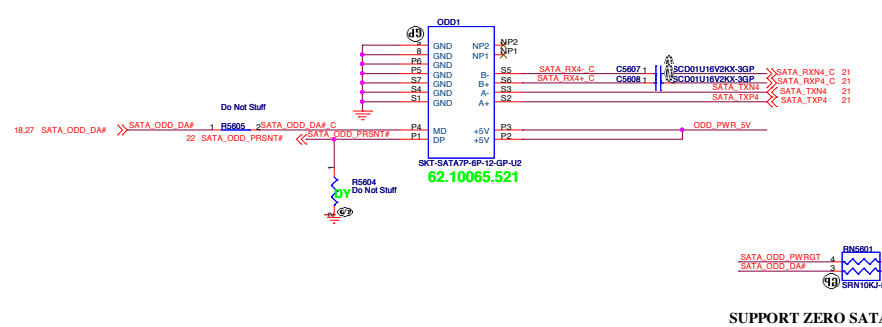
SATA HDD Connector



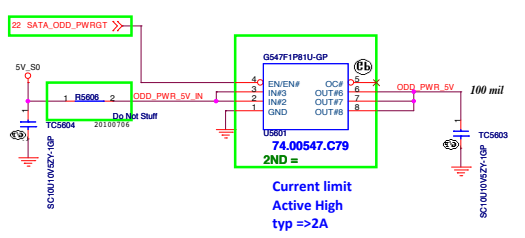
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

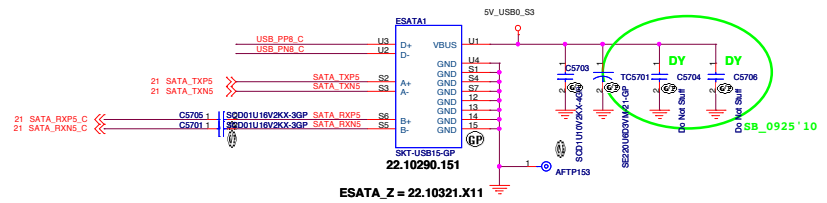
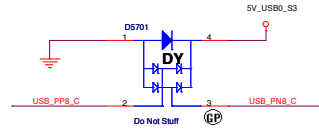
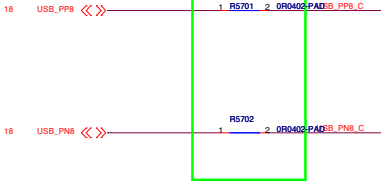
Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD



BOM			
緯創資通 Wistron Corporation			
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
HDD/ODD			
Size	Document Number		Rev
A3	LZ57		-1
Date:	Tuesday, March 28, 2011	Sheet	56 of 102

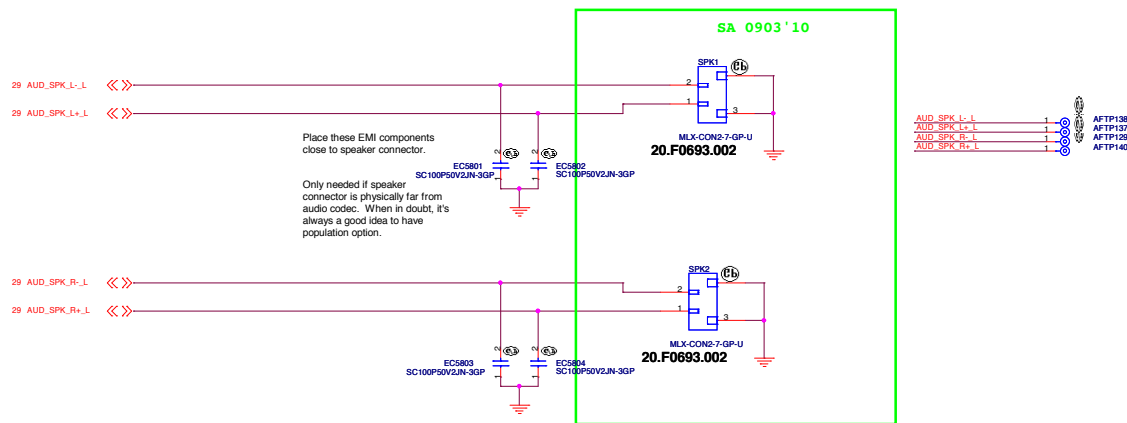


- USB_PNS_C 1 AFTP147
- USB_PPS_C 1 AFTP148
- SATA_TXNS 1 AFTP146
- SATA_TXPS 1 AFTP145
- SATA_RXNS 1 AFTP152
- SATA_RXPS 1 AFTP151
- 5V_USB0_S3 1 AFTP150

BOM

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title E-SATA/USB	
Size A3	Document Number LZ57
Date: Tuesday, March 29, 2011	Rev -1
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INTERNAL STEREO SPEAKERS

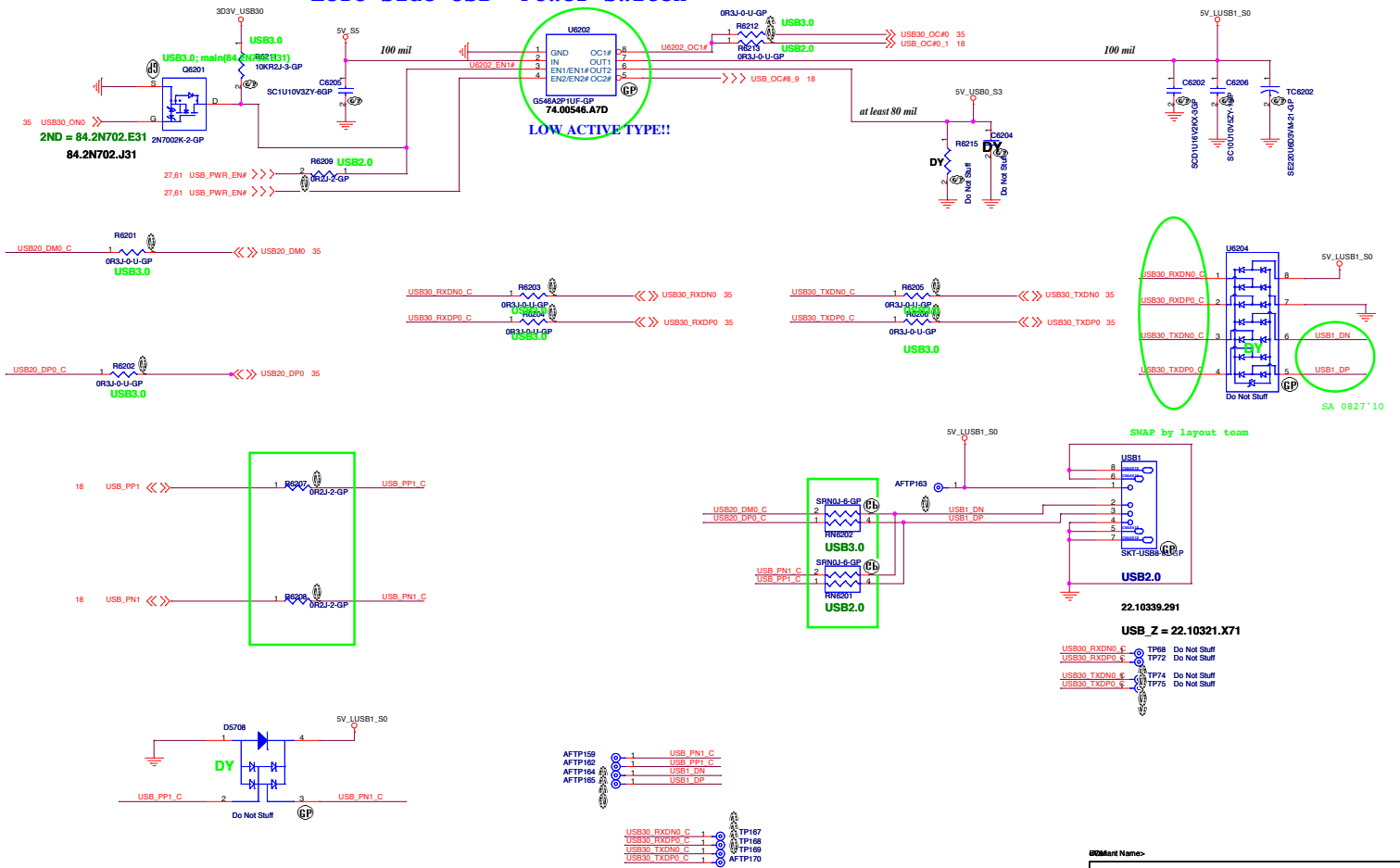


BOM			
緯創資通		Wistron Corporation	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MIC/SPEAKER/AUDIO JACK			
Size	Document Number	Rev	
A3	L757	-1	
Date: Tuesday, March 29, 2011		Sheet	58 of 102

Reserved

BOM		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A3	LZ57	-1
Date	Tuesday, March 25, 2014	
	Sheet	59 of 102

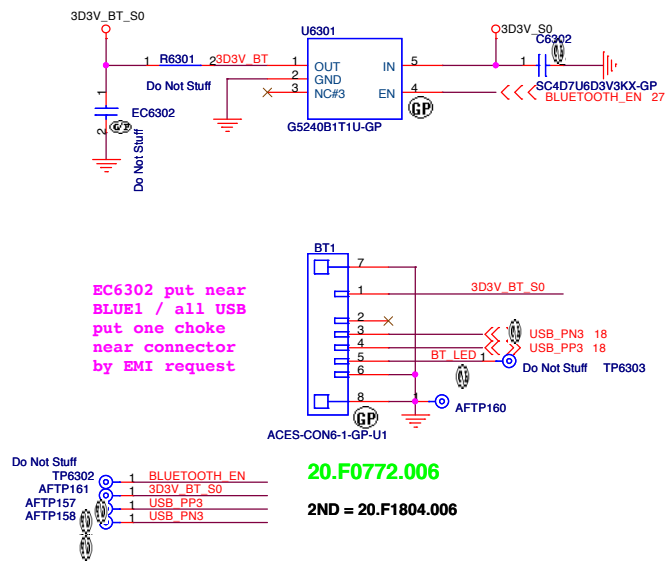
Left Side USB Power Switch



Form Name: Name>		緯創資通 Wistron Corporation 21F, Bld, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 2.0/3.0 Port L757			
Size A3	Document Number		Rev -1
Date	Issued by	Sheet	of
1/2008	MARCO TSAI	62	102

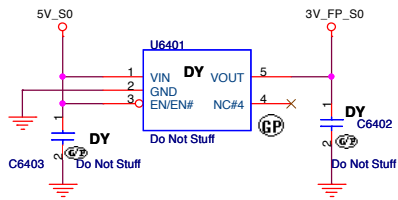
SSID = User.Interface
Bluetooth Module conn.

Bluetooth Module



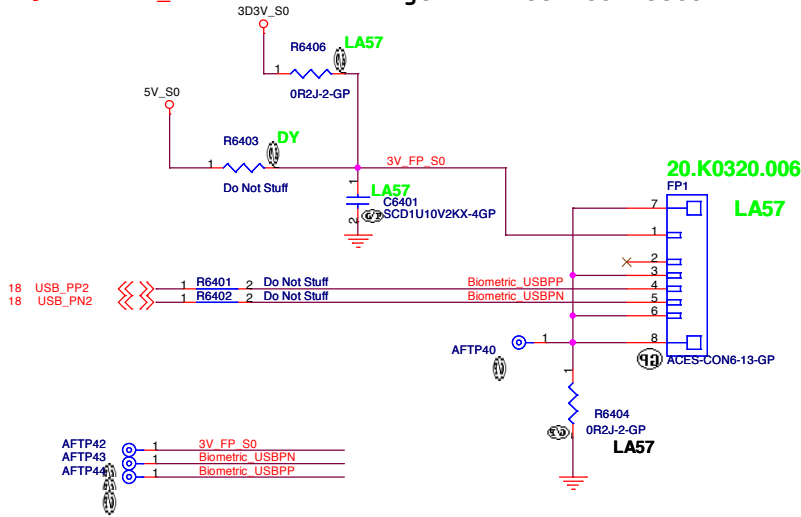
BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Bluetooth			
Size A4	Document Number LZ57		Rev -1
Date:	tuesday, March 29, 2011	Sheet 63 of	102



LA47 change to 3D3V_S0

Finger Printer Connector

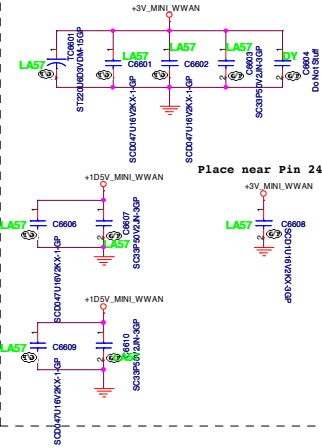


BOM

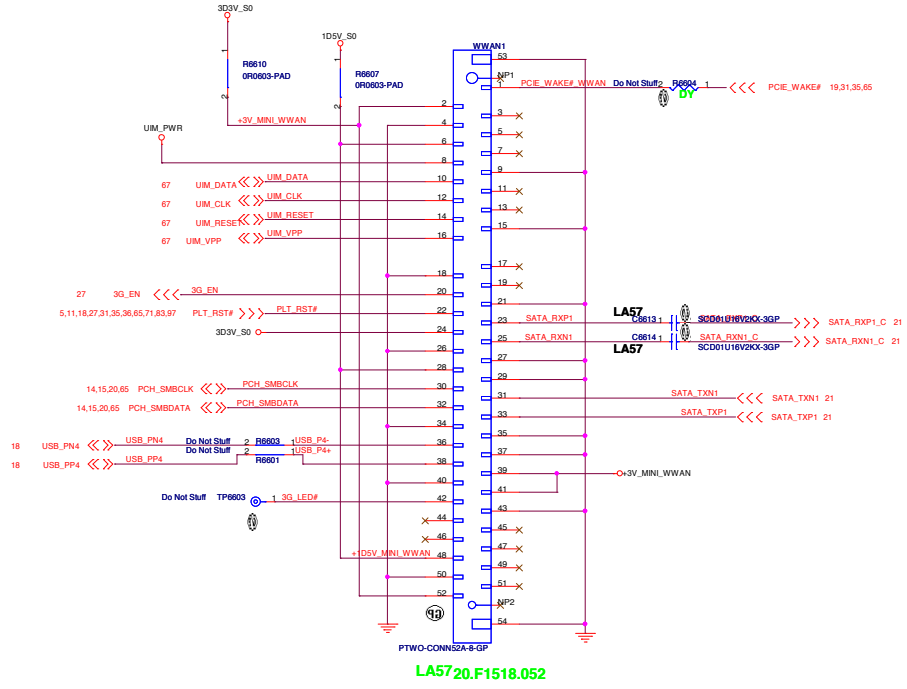
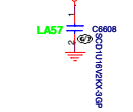
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size A4	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011		Sheet 64 of	102

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



LA5720.F1518.052

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size

Document Number

LZ57

Rev

-1

Date:

Tuesday, March 29, 2011

Sheet

66

of

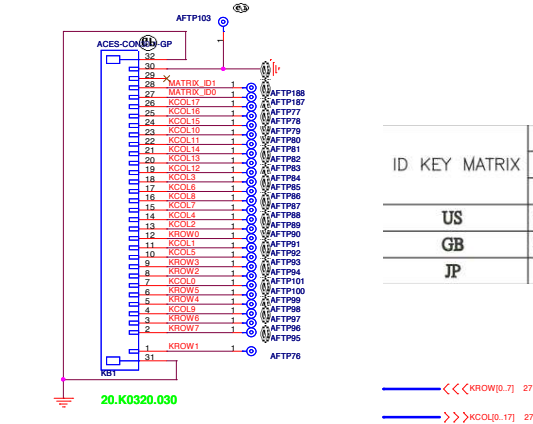
102



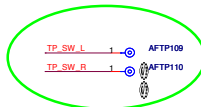
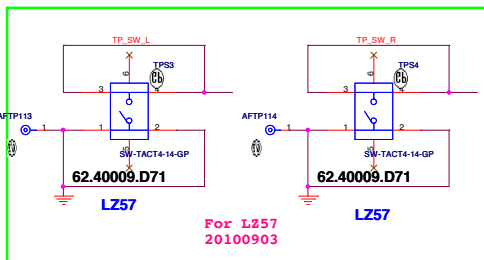
Title			
SIM CARD			
Size A3	Document Number		Rev
	LZ57		-1
Date:	Tuesday, March 29, 2011	Sheet 67 of	102

SSID = KBC

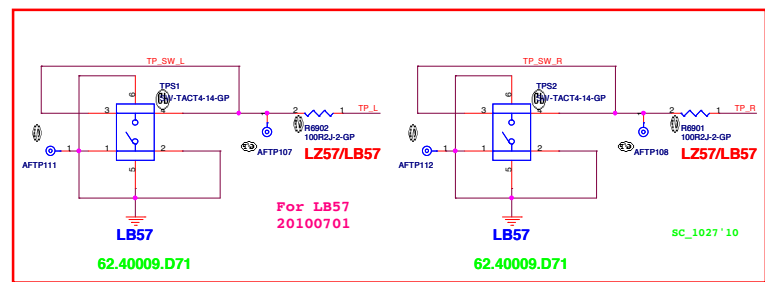
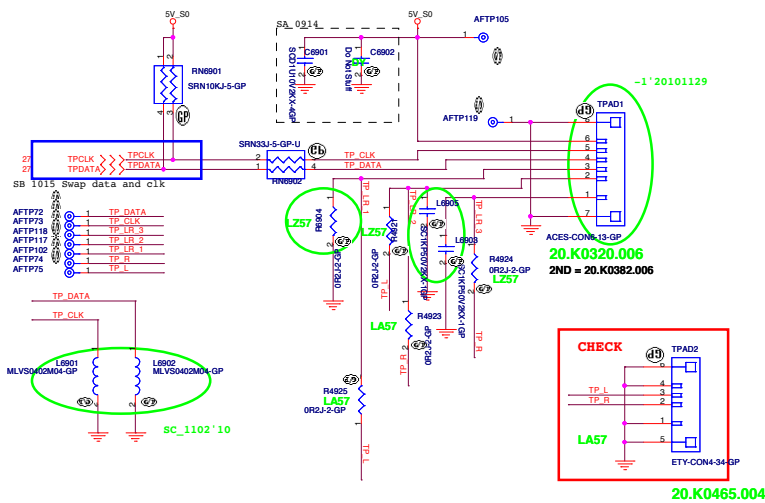
Internal Keyboard Connector



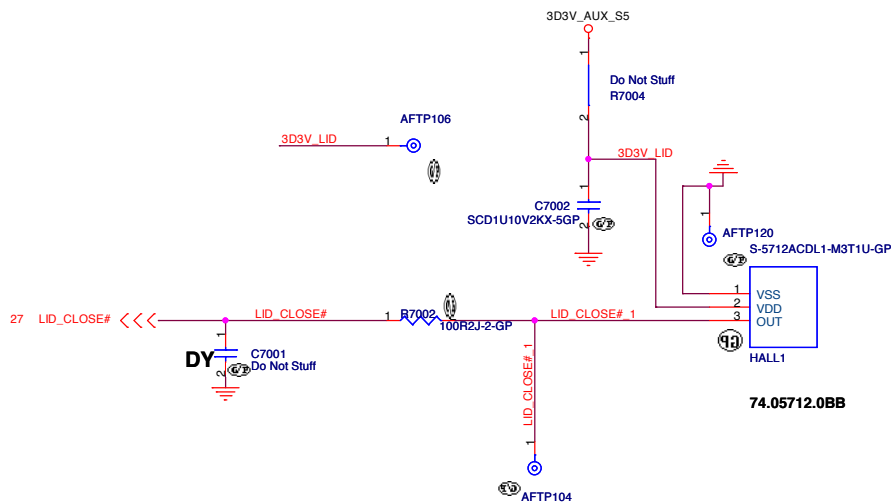
ID KEY MATRIX	SENSE			
	27	28	29	30
US	ID0	ID1	ID2	GND
GB	GND	X	X	GND
JP	X	GND	X	GND



SSID = Touch.Pad

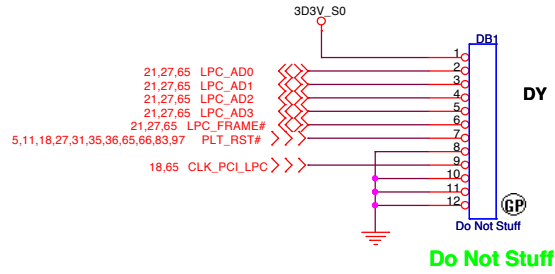


BOM	
緯創資通 Wistron Corporation	
21F, 8th, Sec.1, Hsin-Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Key Board/Touch Pad	
Size	Document Number
A3	LZ57
Date:	Issued: March 28, 2011
Sheet	68 of 102



BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Hall Sensor</div>		
Size <div>A4</div>	Document Number <div>LZ57</div>	Rev <div>-1</div>
Date: Tuesday, March 29, 2011		
2	Sheet 70 of 102	1



BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Dubug connector</div>		
Size <div>A4</div>	Document Number <div>LZ57</div>	Rev <div>-1</div>
Date <div>Tuesday, March 29, 2011</div>	Sheet <div>71</div>	of <div>102</div>

(Blanking)

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Reserved</div>	
Size <div>A4</div>	Document Number <div>LZ57</div>
Date <div>Tuesday, March 29, 2011</div>	Rev <div>-1</div>
Sheet 72 of 102	

(Blanking)

BOM

緯創資通		Wistron Corporation	
21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
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Date: Tuesday, March 29, 2011		Sheet 73 of 102	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>CARD Reader CONN</div>		
Size <div>A4</div>	Document Number <div>LZ57</div>	Rev <div>-1</div>
Date: Tuesday, March 29, 2011		Sheet 74 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>New Card</div>		
Size <div>A4</div>	Document Number <div>LZ57</div>	Rev <div>-1</div>
Date: Tuesday, March 29, 2011		Sheet 75 of 102

(Blanking)

BOM

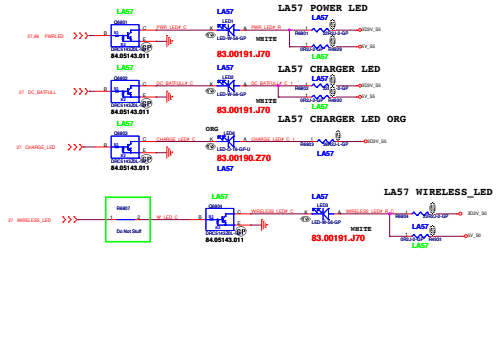
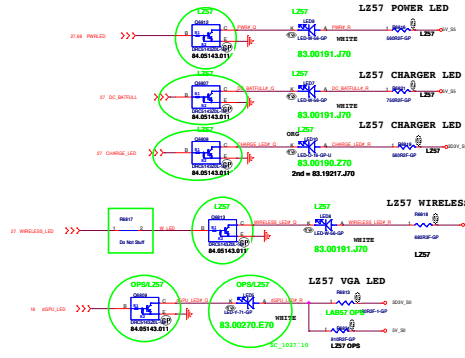
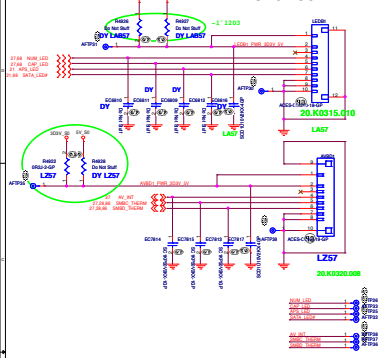
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Title <div>Reserved</div>	
Size A4	Document Number <div>LZ57</div>
Date: Tuesday, March 29, 2011	Rev <div>-1</div>
Date: Tuesday, March 29, 2011	
Sheet 76 of 102	

(Blanking)

BOM

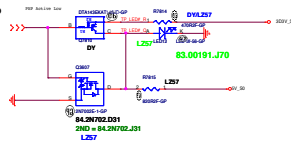
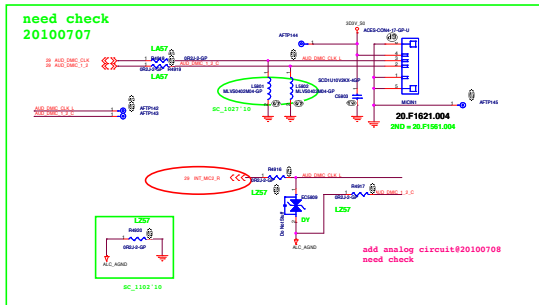
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div> <div>Reserved</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>LZ57</div>		<div>Rev</div> <div>-1</div>
<div>Date: Tuesday, March 29, 2011</div>		<div>Sheet</div> <div>77</div>	<div>of</div> <div>102</div>

LED Bord CONN.

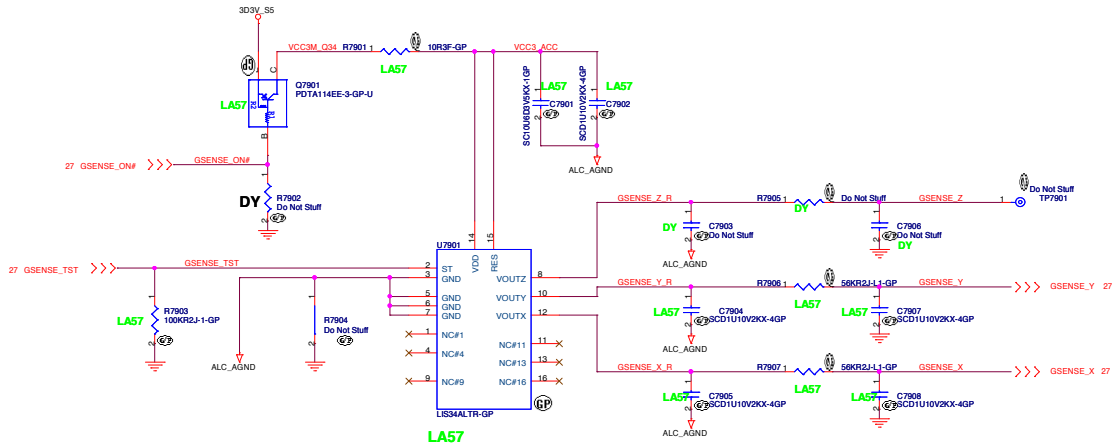


LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic

LZ57 Touch Pad LED



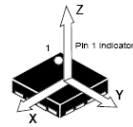
G-Sensor



STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.



	ADXL322	
	LIS244AL	No Accel
	LIS34AL	
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

BOM

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title	
G-Sensor	
Size	
Custom	
Date: Tuesday, March 29, 2011	
Sheet 79 of 102	
Rev	
-1	

(Blanking)

BOM

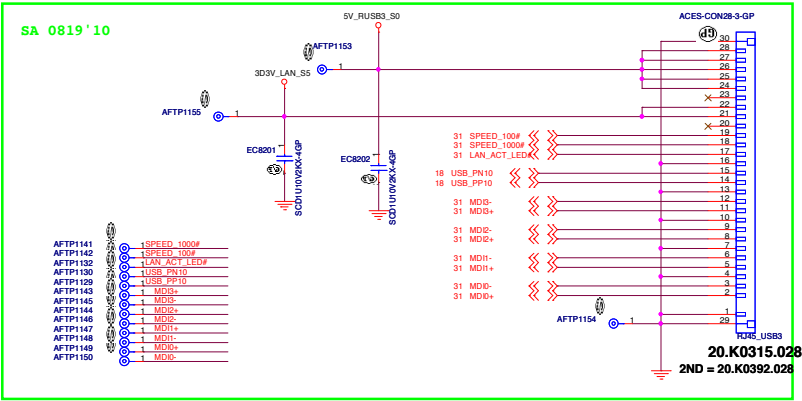
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Reserved</div>	
Size A4	Document Number <div>LZ57</div>
Date Tuesday, March 29, 2011	Rev <div>-1</div>
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(Blanking)

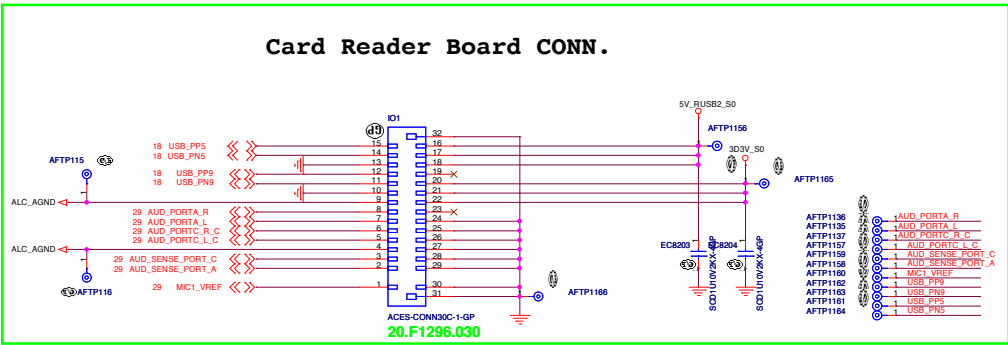
BOM

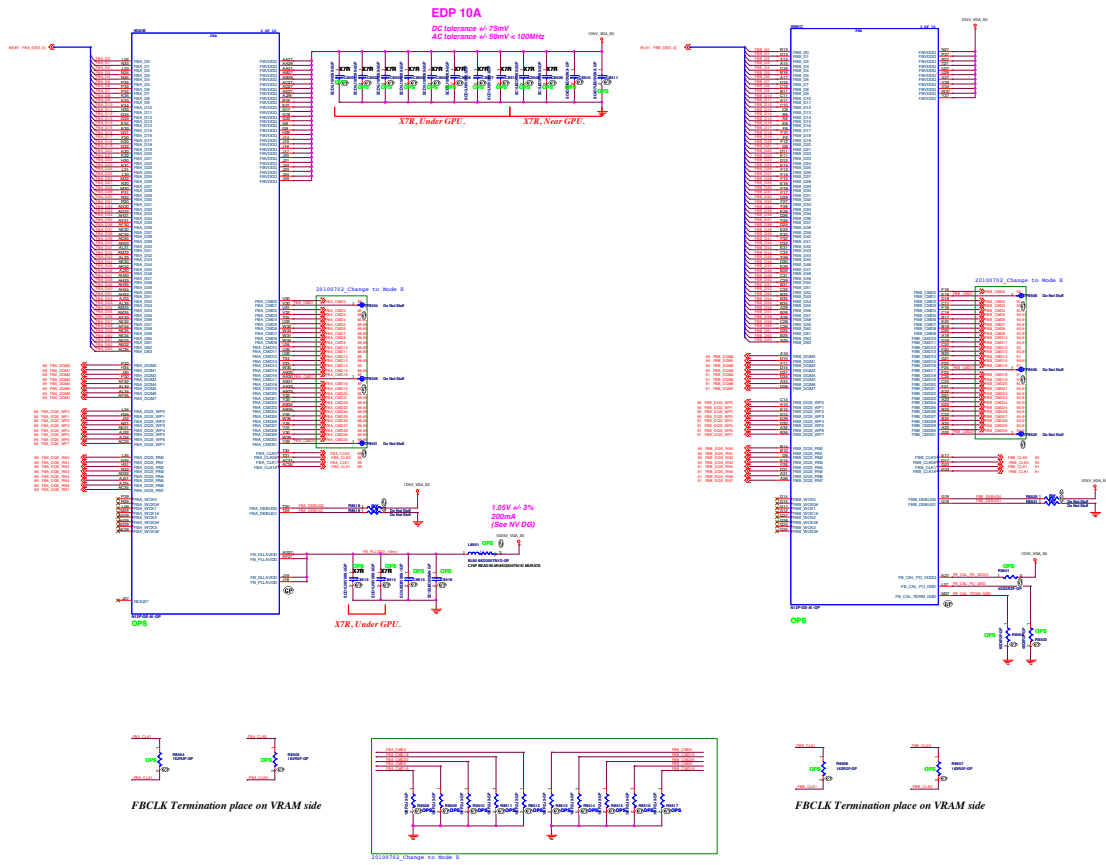
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		<div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>LZ57</div>		<div>-1</div>
<div>Date: Tuesday, March 29, 2011</div>		<div>Sheet</div>	<div>81 of 102</div>

RJ45_USB CONN.



Card Reader Board CONN.

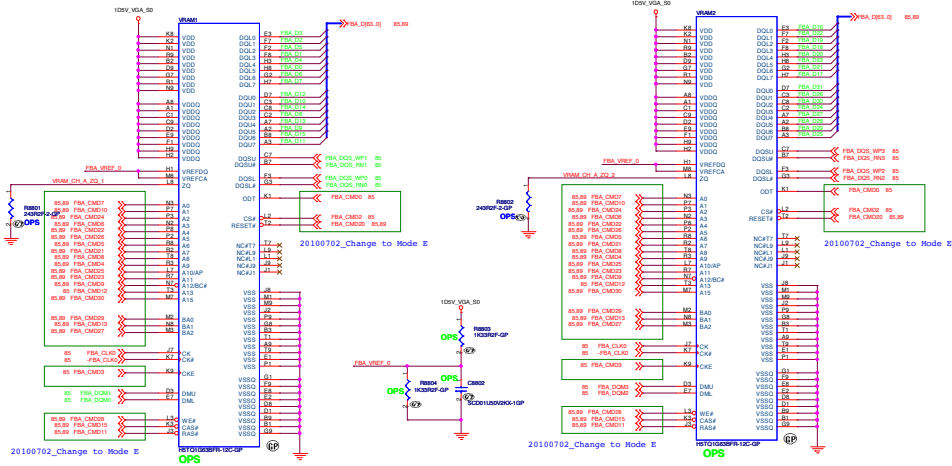




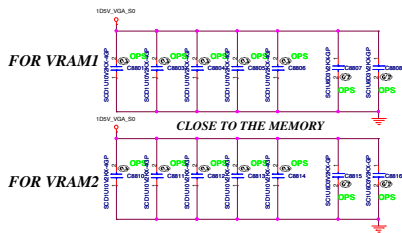


VGA_COPE

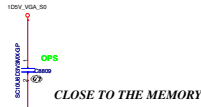




FB CMD mapping Mode D-N12x

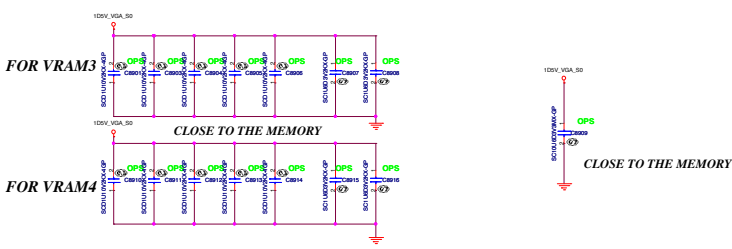
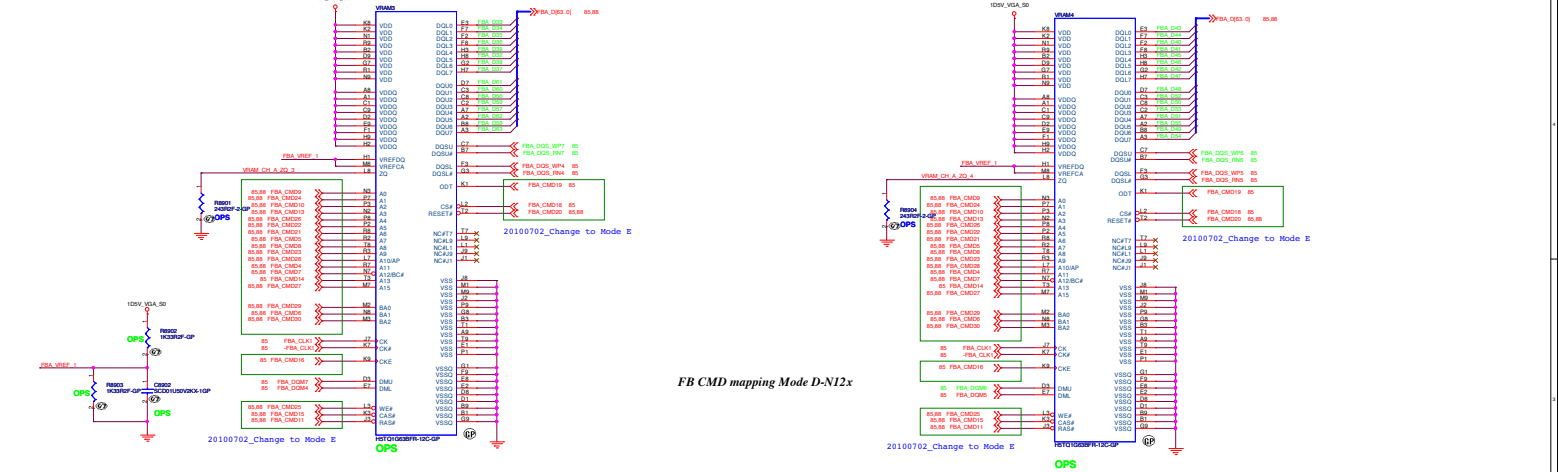


DG requires 4x0.1uF and 8x1.0uF per VRAM chip



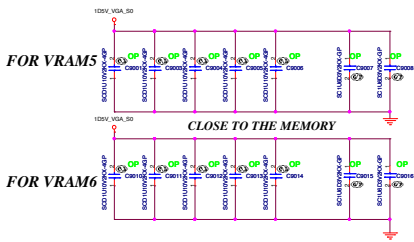
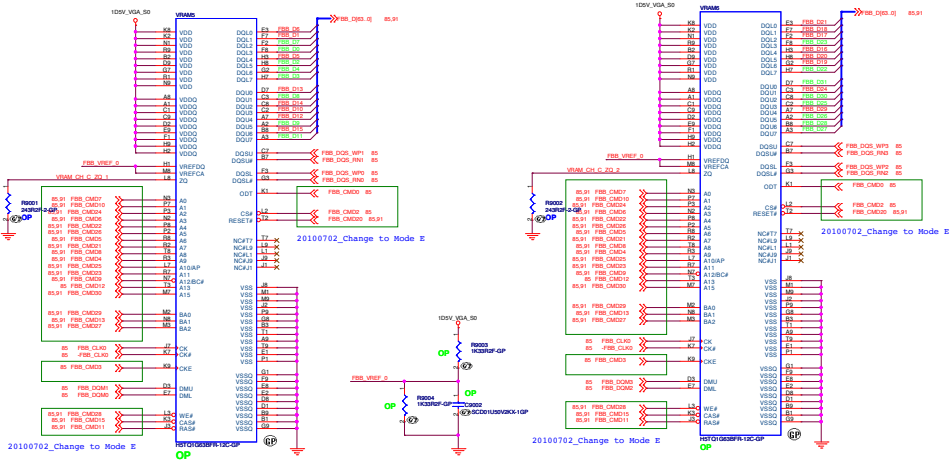
VIDEO FRAME BUFFER PORT A

<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 8F, Sec. 1, Hsin Tai Hsiang Rd., Taichung, Taiwan 40401, Taiwan, R.O.C.</div> </div>	
<div> <div>VRAM CHANNEL-A</div> <div>Document Number</div> <div>LZ57</div> <div>Rev</div> <div>-1</div> </div>	
Rev	1.0
Issue	1.0
Rev	1.0
Issue	1.0



VIDEO FRAME BUFFER PORT A

Wistron Corporation	
101, No. 1, Hsin-Yi Road, Taipei, Taiwan, R.O.C.	
VRAM CHANNEL-A	
Doc. Number	LZ57
Rev.	-1
Date: Tuesday, March 20, 2012	Drawn by: [signature]

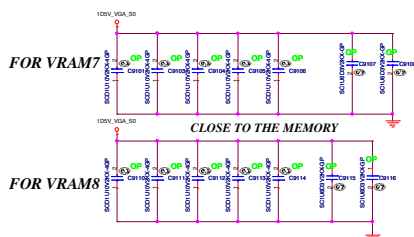
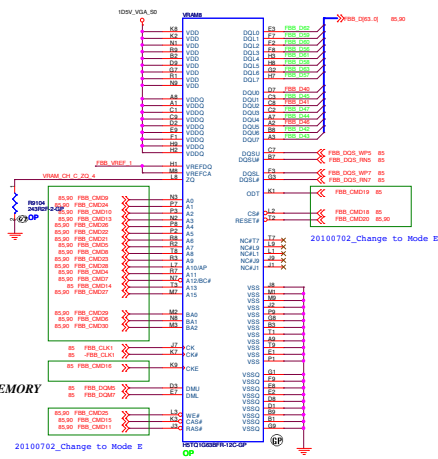
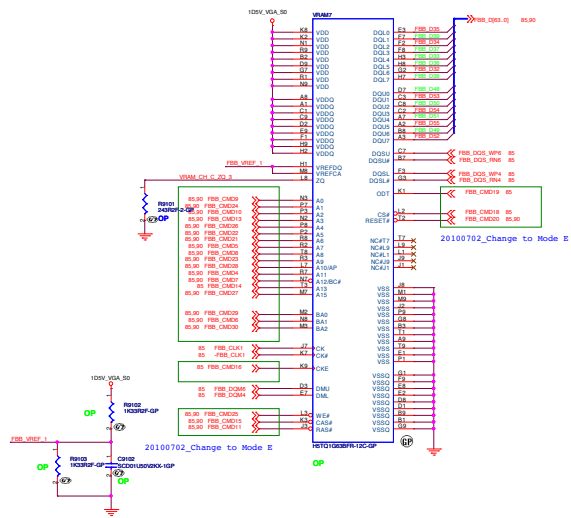


DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

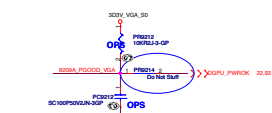
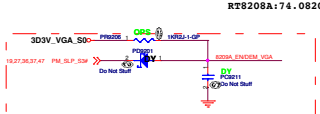
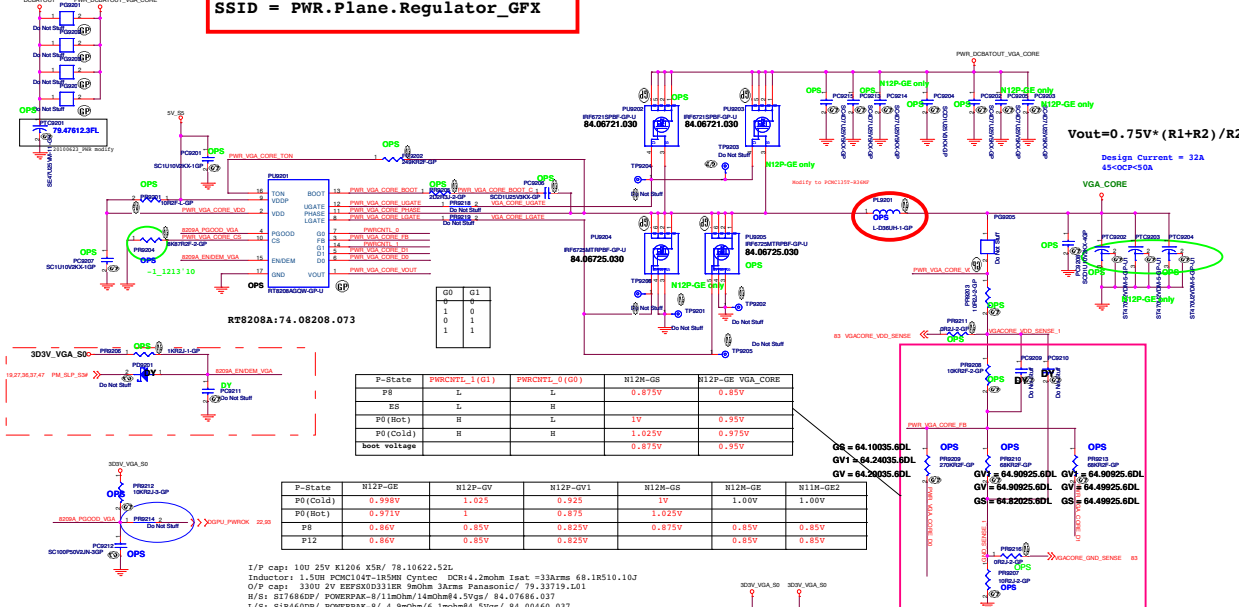
Wistron Corporation	
2/F, No. 1, Hsin-Tai Rd., Tainan, Taiwan, R.O.C.	
VRAM CHANNEL-C	
Document Number	L257
Date	March 29, 2011
Rev	1



VIDEO FRAME BUFFER PORT C

<div> <div>緯創資通</div> <div>Wistron Corporation</div> </div>	
<div> <div>File</div> <div>VRAM CHANNEL-C</div> </div>	
Rev	1.0
Date	2011.03.25
Drawn	01
Check	01
Appr	01

SSID = PWR.Plane.Regulator_GFX



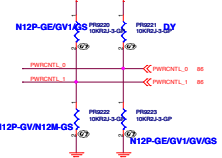
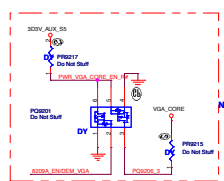
RTS208A:74.08208.073

P-State	PWRCTRL_1(G1)	PWRCTRL_2(G0)	N12P-GE	N12P-GE VGA_CORE
PS	L	L	0.875V	0.85V
ES	L	L	1V	0.95V
FS (Hot)	H	H	1.025V	0.975V
FS (Cold)	H	H	0.875V	0.95V
boot voltage				

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
PS (Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
PS (Hot)	0.971V	1	0.875	1.025V	0.85V	0.85V
FS	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
F12	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V

I/P caps: 10u 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5uH PCHM1047-1R5M Cyntec DCI:4.2mohm Isat =33Arms 68.18510.10J
 O/P caps: 330u 2V KEEF03033328 33mohm 3Arms Panasonic/ 79.33719.1d1
 H/S: S176860P/ POWERPAK-8/11mohm/14mohm/4.5Vgs/ 84.07686.037
 L/S: S18460DP/ POWERPAK-8/ 4.9mohm/6.1mohm/4.5Vgs/ 84.00460.037
 Switching freq-->350KHz

Frequency setting
 470K -->165KHz
 200K -->323KHz
 100K -->500KHz



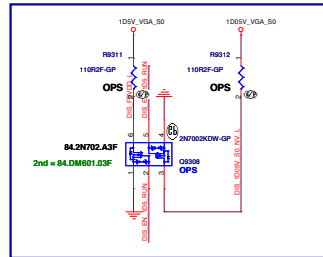
	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
PS (Cold)	0.998V	0.946V	1.048V	
PS (Hot)	0.971V	0.915V	1.011V	
FS/F12	0.86V	0.835V	0.86V	
Boot Voltage	0.971V	0.915V	0.840V	
PS209	270K(64.27035.6DL)	240K(64.24035.6DL)	200K(64.20035.6DL)	
PS210	68K(64.68025.6DL)	49.9K(64.49925.6DL)	68K(64.68025.6DL)	
PS213	68K(64.68025.6DL)	49.9K(64.49925.6DL)	49.9K(64.49925.6DL)	

The schematic shows the I2C bus termination circuit for the AD9680. It includes the following components and connections:

- AD9680 Pin 17 (SDA):** Labeled "I=30mA". It has pins for VDD, GND, IN, NC/VOUT, and OUT.
- AD9680 Pin 18 (SCL):** Labeled "DO NOT STUFF DY". It has pins for VDD, GND, IN, NC/VOUT, and OUT.
- Termination Resistor R3009:** A 22Ω resistor connected between SDA and SCL.
- Resistor R3008:** A 1kΩ resistor connected from SDA to ground.
- Resistor R3007:** A 1kΩ resistor connected from SCL to ground.
- Capacitor C3007:** A 0.01μF capacitor connected from SDA to ground.
- Capacitor C3008:** A 0.01μF capacitor connected from SCL to ground.
- Labels:** "DOPU_PWK_TO DEV" and "DOPU_PWRC 22.82" are present near the top right.

Below the schematic, there is a note about the ramp up rail:

1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

[illegible][illegible]

(Blanking)

(Blanking)

BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CRT Switch	
Size	Document Number	Rev	
A3	LZ57	-1	
Date:	Tuesday, March 29, 2011	Sheet	95 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TOUCH PANEL			
Size A4	Document Number LZ57		Rev -1
Date:	Tuesday, March 29, 2011	Sheet 96 of	102

CPU Plate

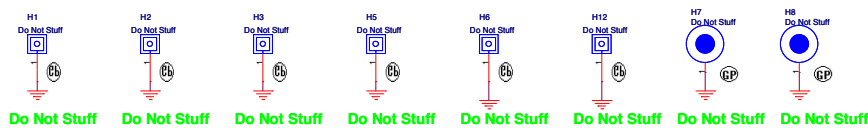
VGA Std-Off

Check test point

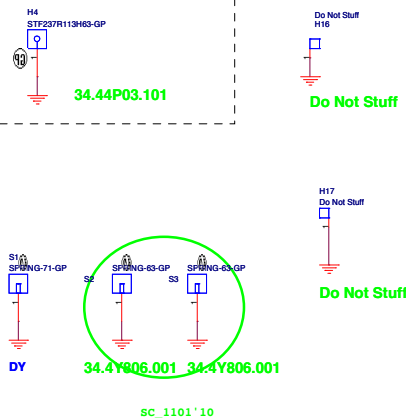


Test Point放在Dimm Door打開可量測處

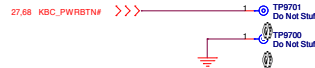
Structure boss



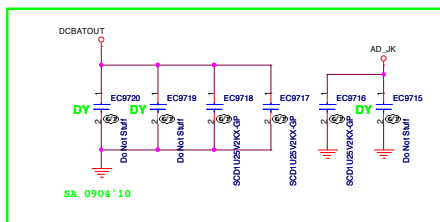
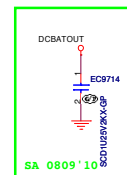
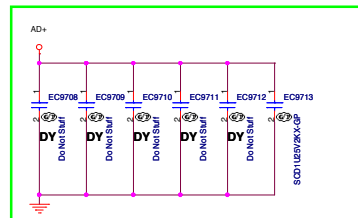
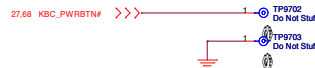
MiniPCI Std-Off



POWER TESTING POINT--TOP



POWER TESTING POINT--Bottom



BOM

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsein 221, Taiwan, R.O.C.

Title
 Size K3
 Date: 1/25/2011
 Document Number
 L757
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 Rev -1

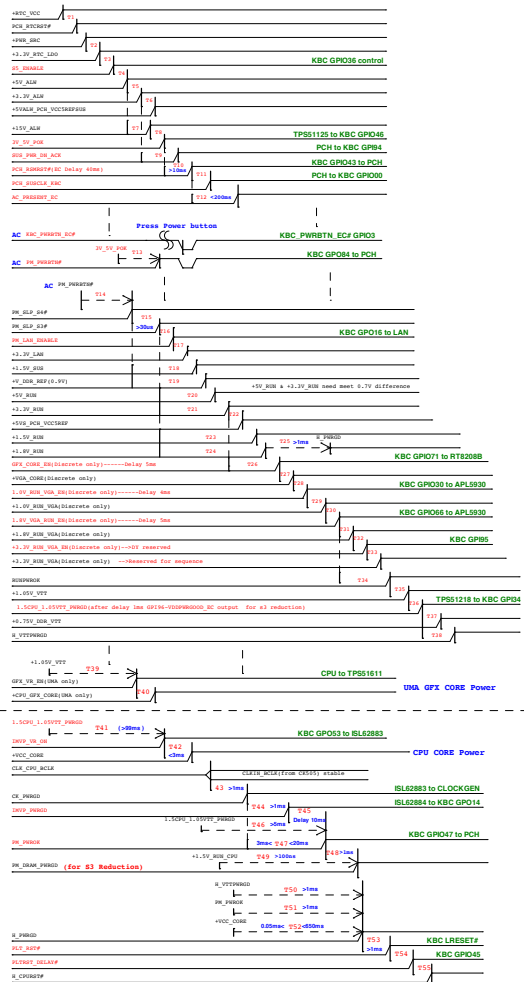
(Blanking)

BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
Change History	
Size	Document Number
A4	LZ57
Date:	Rev
Tuesday, March 29, 2011	-1
2	Sheet 98 of 102

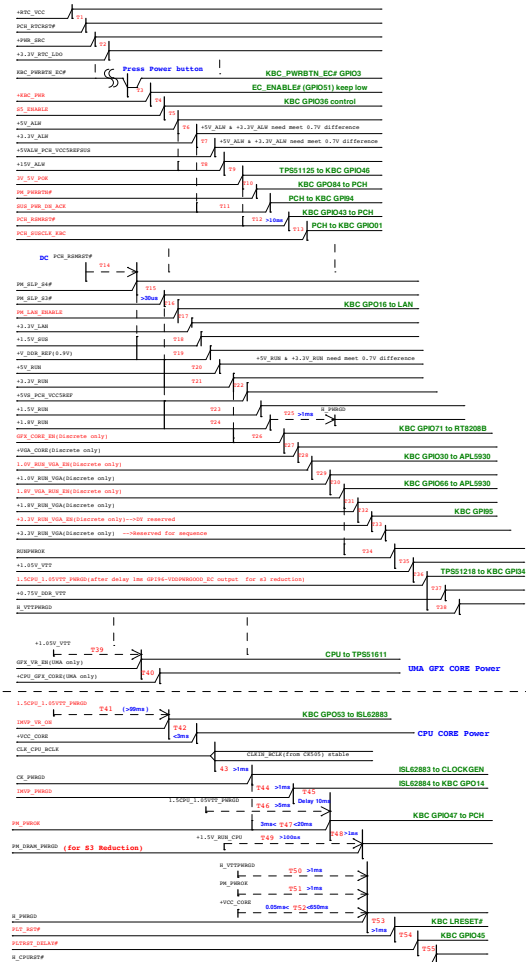
(AC mode)

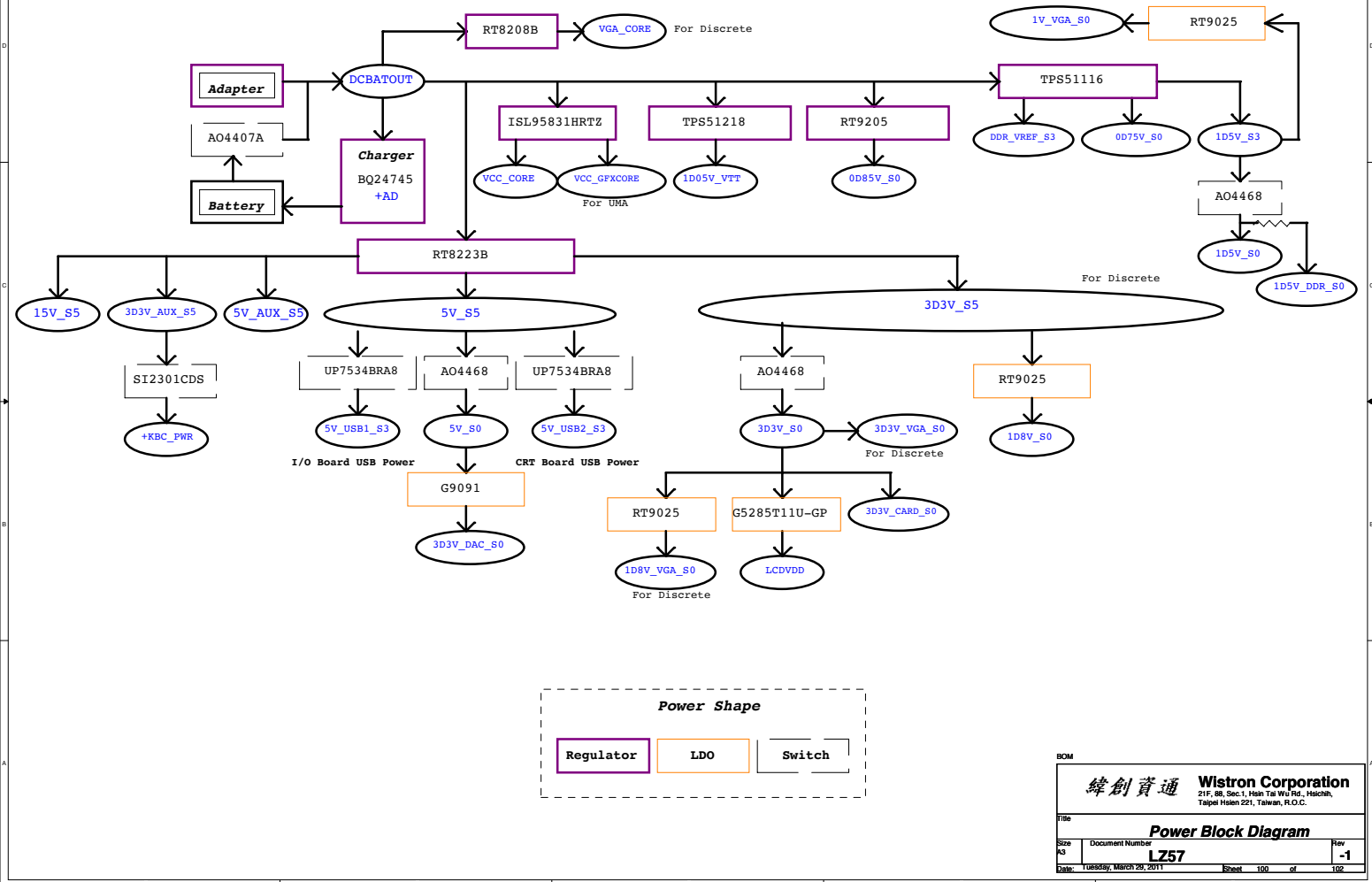
red word: KBC CPIC



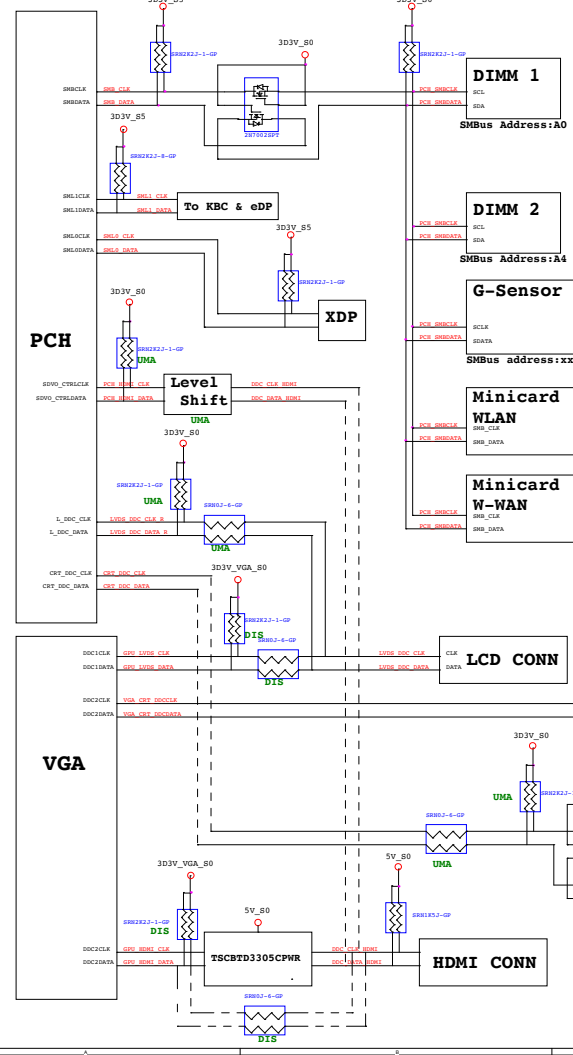
(DC mode)

red word: XBC GPIC

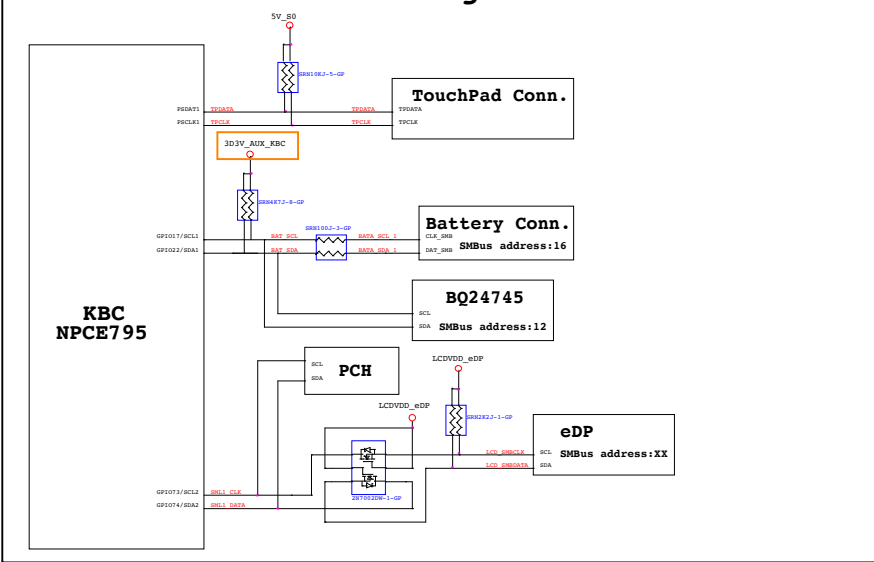




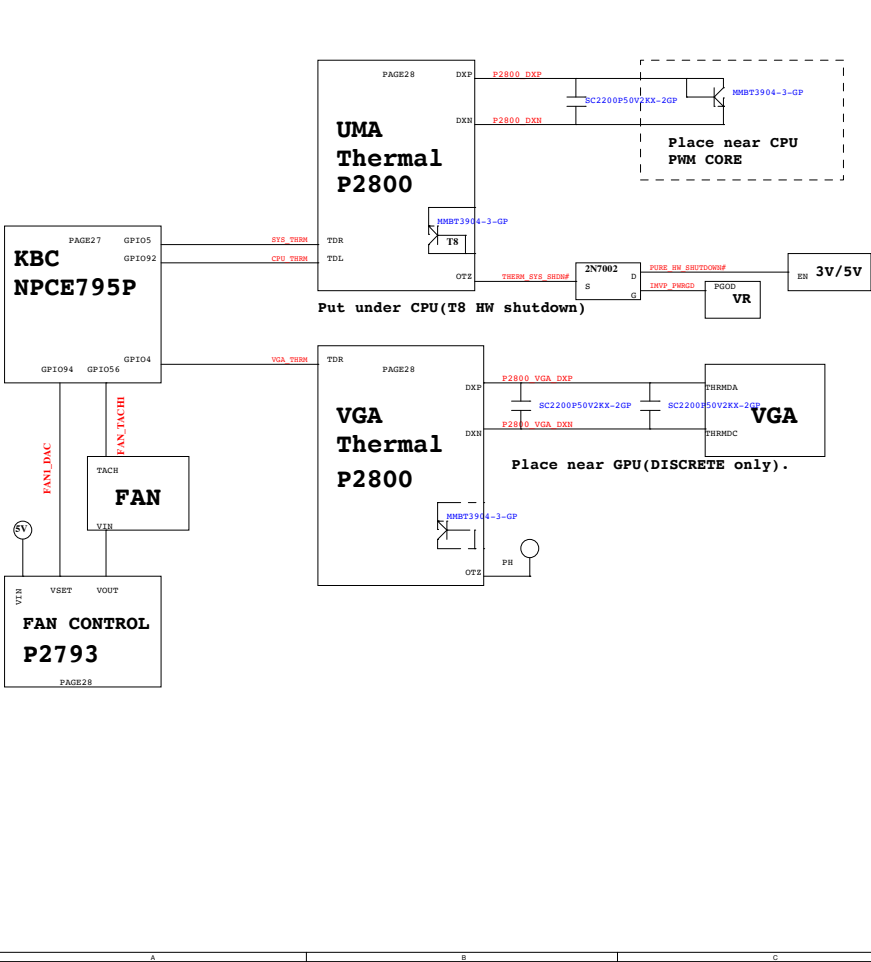
PCH SMBus Block Diagram



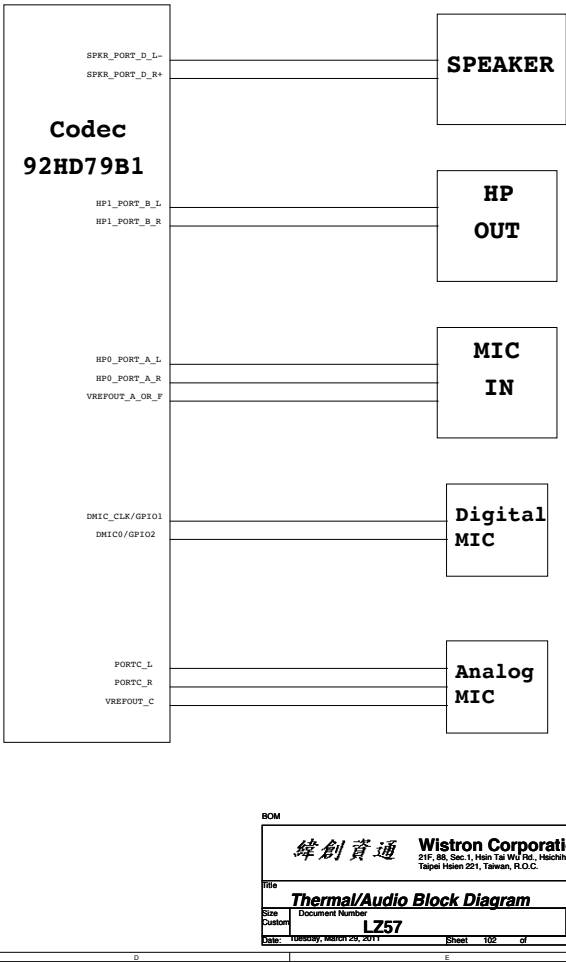
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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				21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Thermal/Audio Block Diagram			
Size	Document Number				Rev
Custom	LZ57				-1
Date: 1/26/2011, March 23, 2011		Sheet	102	of	102